

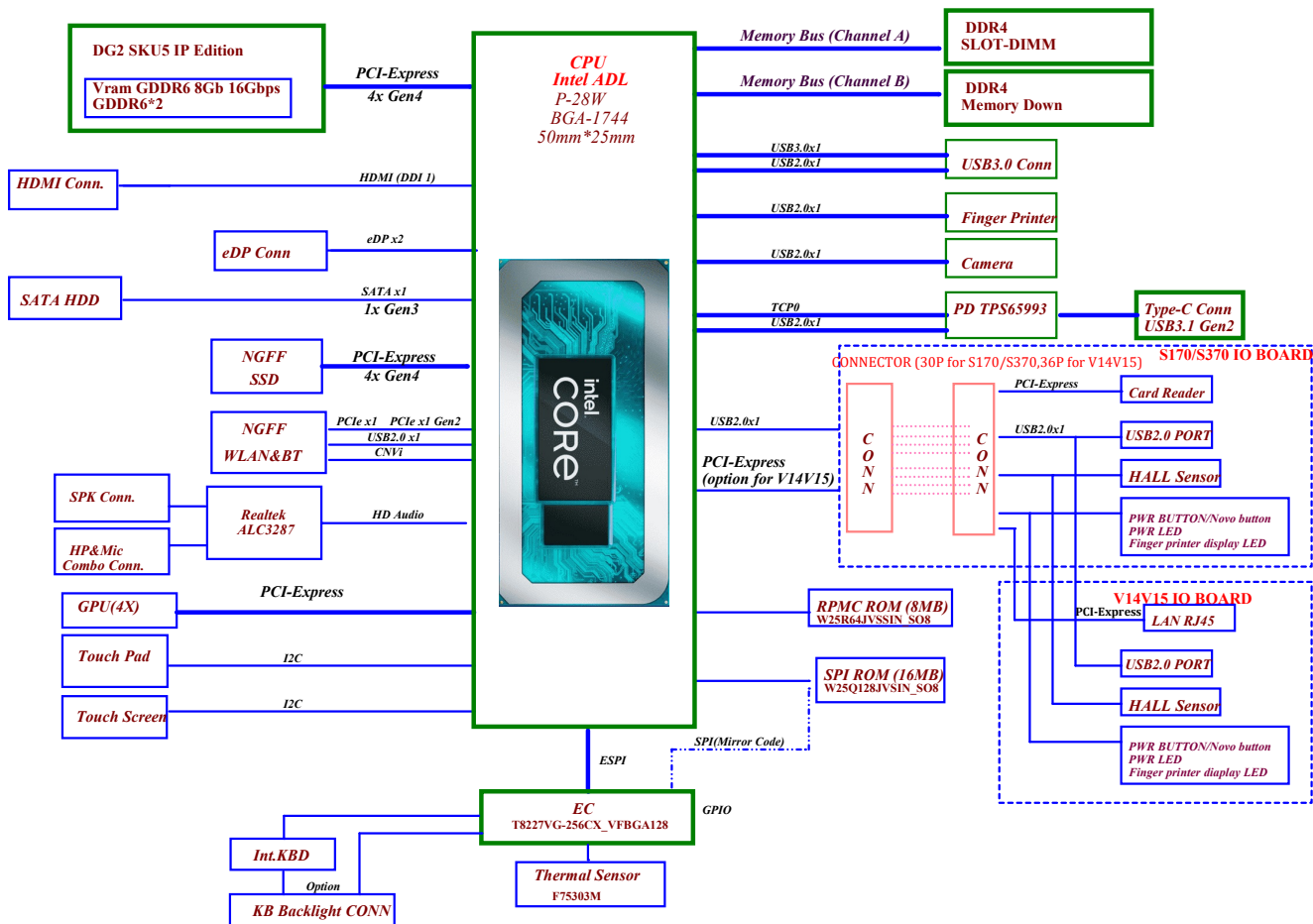
LCFC NM-E341

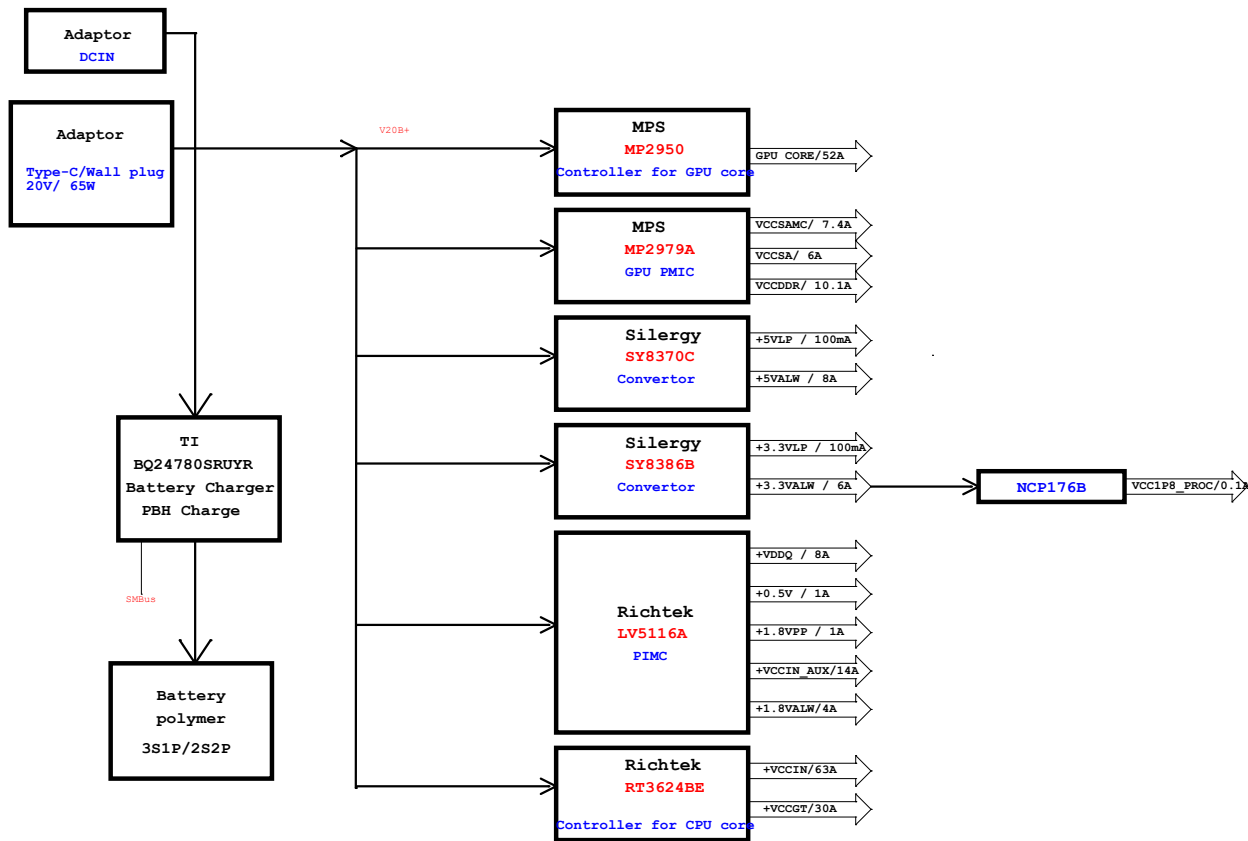
JS473&JS573&JS478&JS578&JS778 S170/S370 MB Schematics Document

Alder Lake P with DDR4 + Slot-DIMM

REV: 0.1
2021-02-18

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				Cover Page	
				Date: Friday, February 18, 2022 Sheet 1 of 130	





Voltage Rails (O --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>				
	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTB +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory DMM	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WLANX
EC_SMB_CK1	IT8586E	V	V	X	V	X	X	X	X	X	X
EC_SMB_DA1	+3VL_EC				+3VL_EC						
EC_SMB_CK2	IT8586E	X	X	V	V	X	V	X	X	V	X
EC_SMB_DA2	+3VS			+3VL_AGN	+3VS		+3VALW_PCH				
EC_SMB_CK3	IT8586E	X	X	X	V	X	X	V	X	X	X
EC_SMB_DA3	+3VL_EC				+3VL_EC						
PCH_SMB_CLK	PCH	X	X	X	X	X	V	X	V	X	V
PCH_SMB_DATA	+3VALW_PCH						+3VALW_PCH		+3VS		+3VS

EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	not use		DOR4.SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			WLAN	Reserved
						DGPU	need to update

GPU PWR Controller need to update

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

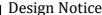
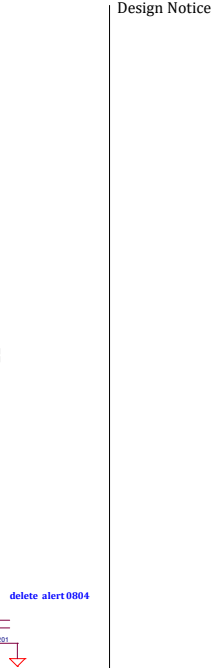
HSIO PORT	Function
USB3.0	1 USB3.0 Comm
	2 USB3.0 Comm
	3 NC
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Comm
	2 NC
	3 USB3.0 Comm
	4 USB2.0 comm
	5 Card reader
	6 Touch Screen
	7 Camera
	8 NC
	9 NC
	10 Bluetooth
PCIE	5-8 X4 DGPU
	9 WLAN
	10 NC
	11 SATA HDD
	12 NC
	13-16 X4 PCIE/SATA SSD

Re-Driver

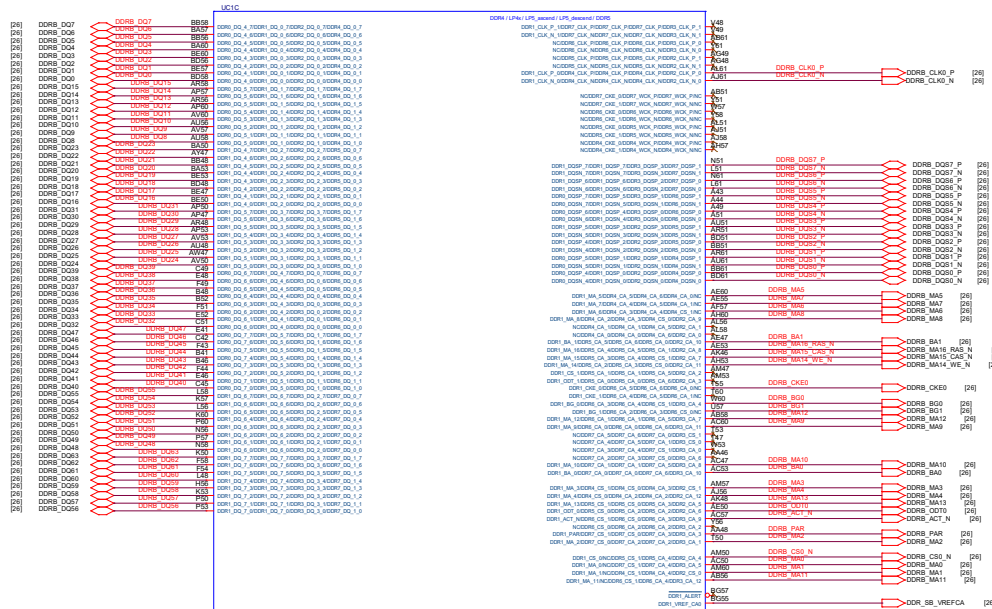
25W

WIMI Royalty

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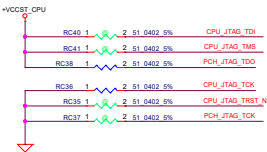
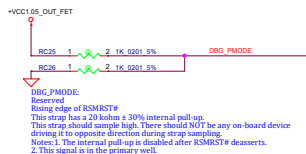


Title	S170/S370-IAL	LCFC
Size C	Document Number P008-CPU (2/16) : (LPDDR4X-CF	R
Date	Release Date	Sheet

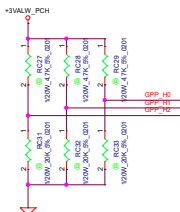
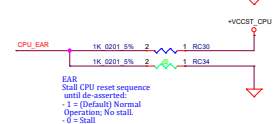
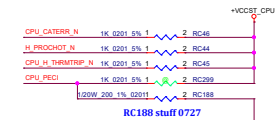
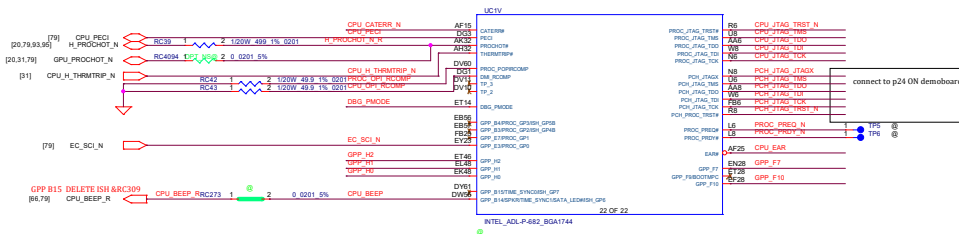


delete alert 0804

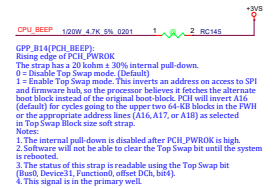
Debug usage



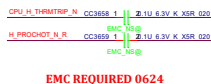
Design Notice



GPP_H0: Boot Strap 1
GPP_H1: Boot Strap 2
GPP_H2: Boot Strap 3
GPP_H3: Boot Strap 4
These straps have a 20 kohm ± 30% internal pull-down.
This strap has a 20 kohm ± 30% internal pull-up.
These are bit [2:1] of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_CS) for the encoding.
Notes: 1. The internal pull-down is disabled after RSMRST# deasserts.
2. This signal is in the primary well.
* 0000 = Master Attached Flash Configuration (BIOS / CSM on SPI), eSPI is enabled
0010 = Master Attached Flash Configuration (BIOS / CSM on SPI), eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSM on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / CSM on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSM on slave attached SPI.

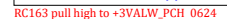



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				1	P0120-CPU(4,16) : MISC/JTAG
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				Rev	1.0

Card Reader
OR LAN

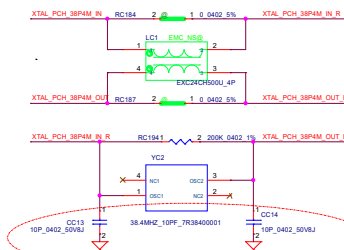



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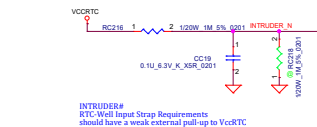
GPU_CLKREQ3_N pull high to 3VS or 3VALW_PCH?



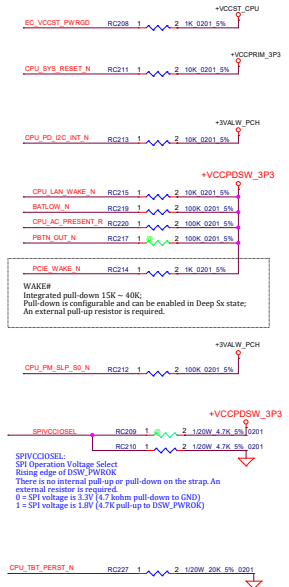
Crystal



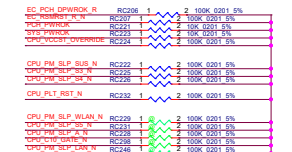
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			Date Friday, February 18, 2022	Sheet 96 of 110



Design Notice



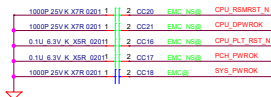
GP07(BB_TBT_PERST#):
 Reserved
 Rising edge of DSW_PWROK
 This signal has a 20K+30% internal pull-down.
 This strap should sample LOW. There should NOT be any on-board device
 driving it to opposite direction during strap sampling
 Notes:
 1. The internal pull-down is disabled after DSW_PWROK is high.
 2. This signal is in the DSW well




Glitch Free Requirements:
Pull-up resistor is required if a device is monitoring SLP_S0#
before RSMRST# de-assertion

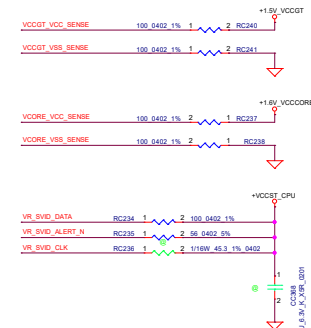
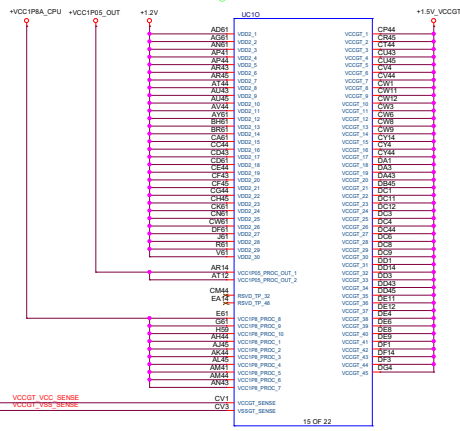
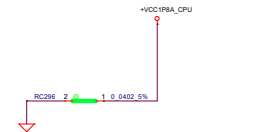
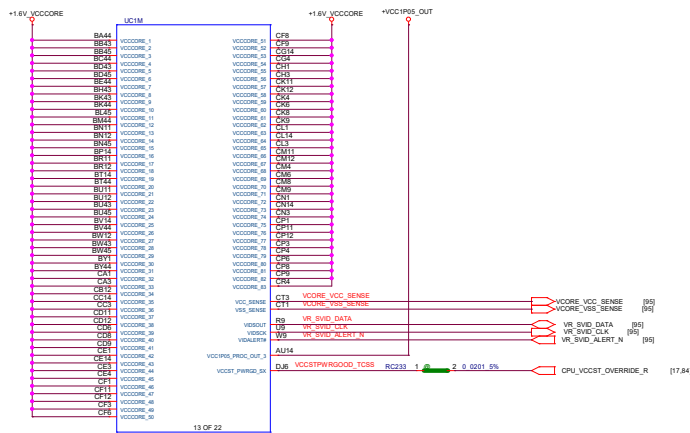
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode

EMC/RF Required

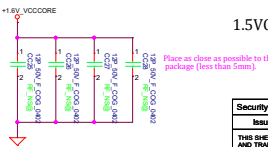
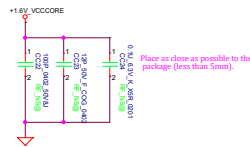


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			P017-CPU(11/16) : SYSTEM PM	1.0

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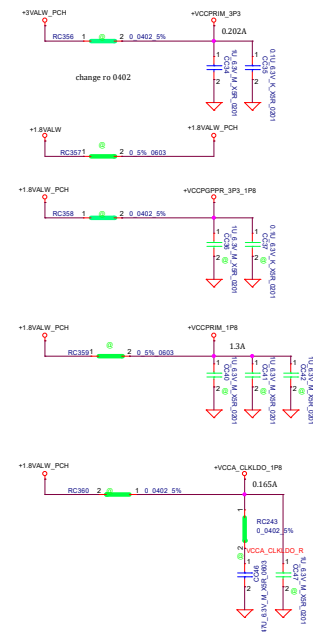
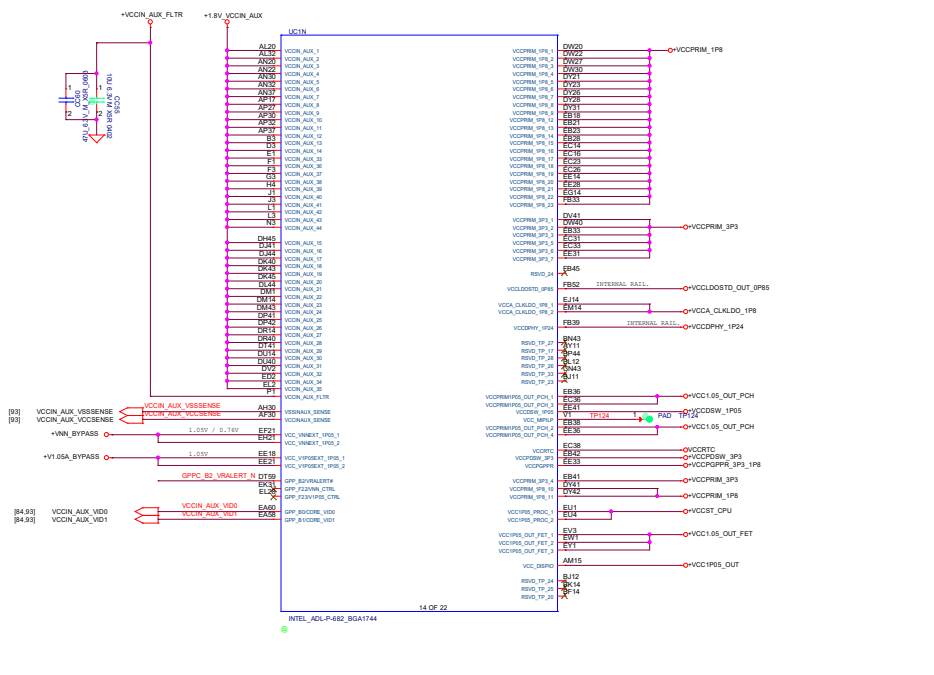
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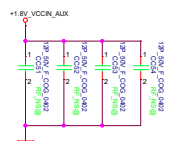
1.5VCCGT ADD RF C?


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				18	P018-CPU (12/16) : CPU Power (1/2)
				Date	Friday, February 18, 2022
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Design Notice



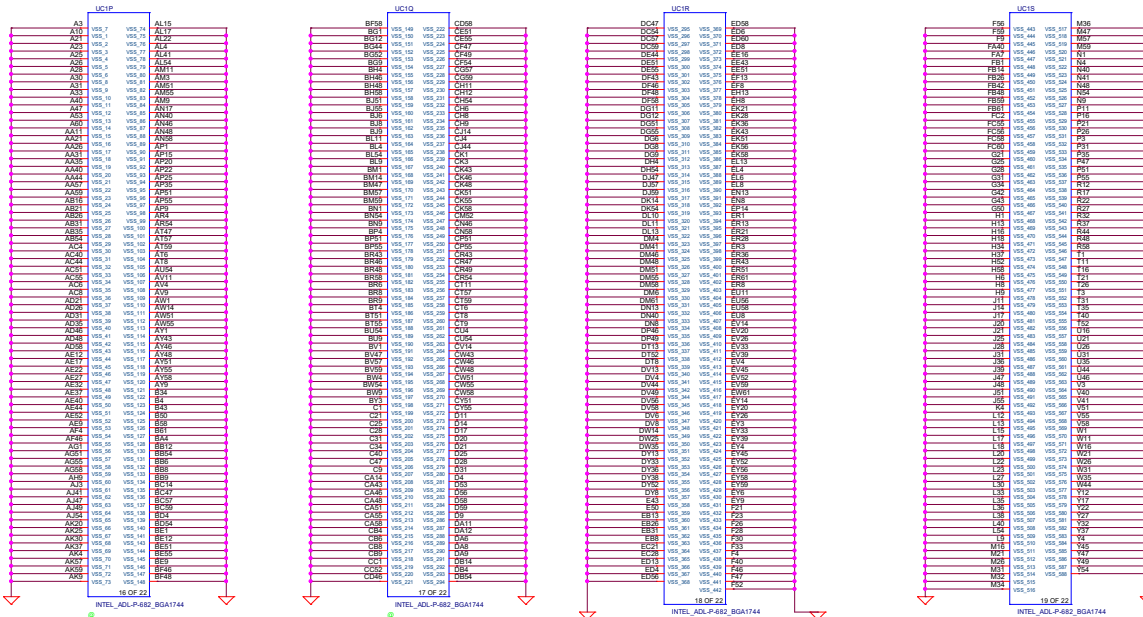
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Doc. Number	Rev.
P020-CPU(14/16) : PCH Power	1.0



UC10

AP21

AK28

AK28

AL30

AL30

BD41

BD41

DT40

EL40

EF38

EH40

RSID_1

RSID_2

RSID_3

RSID_5

RSID_7

RSID_9

RSID_9

RSID_10

RSID_13

RSID_15

RSID_16

RSID_20

4 OF 22

INTEL_ADL-P-682_BGA1744

6

ADD CFG 15 FOR PCIE 4X PORTB

DELETE CFG1,3,4,7

CFG STRAPS for CPU

Reserved configuration lane	
CFG[1:0]	N/A
PCI Express® Static x8 Lanes Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.
Reserved configuration lane	
CFG3	N/A
Reserved	
CFG4	N/A
PCI Express® Bifurcation	
CFG[6:5]	N/A
Reserved configuration lane	
CFG[13:7]	N/A
PEG60 Lane Reversal	
CFG14	★ 1 = (default) normal 0= Reversed
PEG62 Lane Reversal	
CFG15	★ 1 = (default) normal 0= Reversed
Reserved configuration lane.	
CFG[17:16]	N/A

Signal Name Description
Vss Ground: Processor ground node
Vss NCTP Non-Critical To Function: These signals are for package mechanical reliability and should not be connected on the board.
RSVD Reserved: All signals that are RSVD should not be connected on the board.
RSVD_NCTP Reserved Non-Critical To Function: RSVD_NCTP should not be connected on the board.
RSVD_TP Test Point: Intel recommends to route each RSVD_TP to an accessible test point. Intel may require these test points for platform specific debug. Leaving these test points inaccessible could delay debug by Intel.

PDG page319

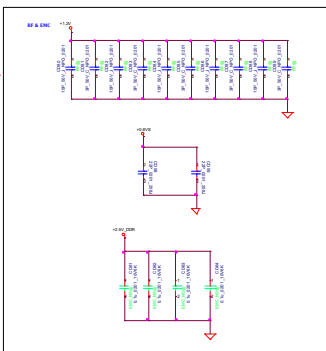
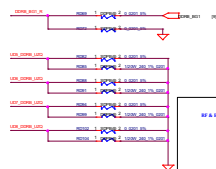
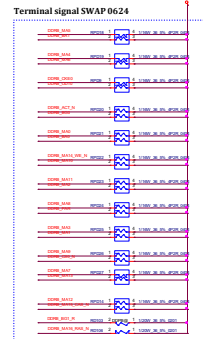
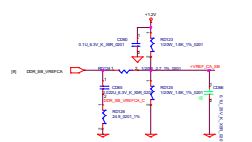
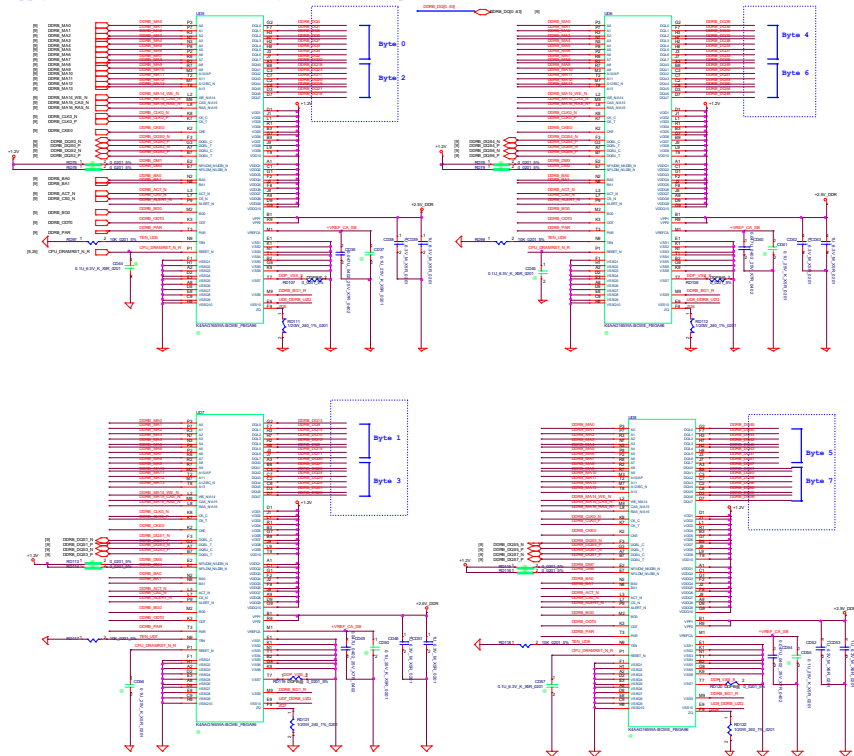
CFG[10:9] PU: Ensure reliable boot across HVMM

TABLE : Functional Strap

GPP_B18/GSPID0_MOSI (No Reboot)	R563
HIGH Enable "No Reboot" Mode	ASM
LOW Disable "No Reboot" Mode (Default)	NO ASM

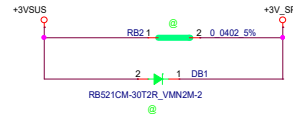
LOGIC









Apply X76 BOM to control SDP Memory Down stuff components!



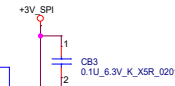
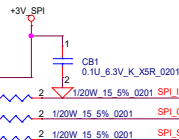
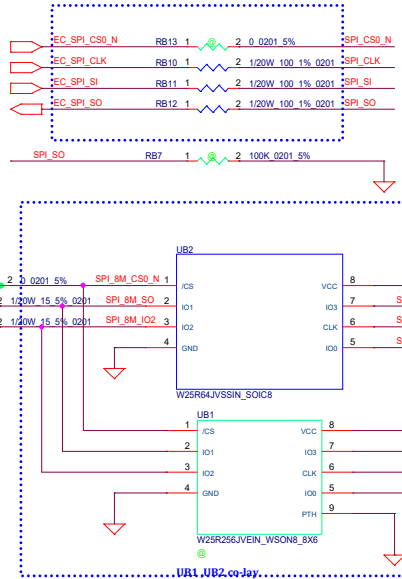
RB3,4,5,6,8CHANGE TO 00HM

[11]	CPU_SPI0_CS0_N	CPU_SPI0_CS0_N	RB1	1	2	0	0201	5%	SPI_CS0_N
[11]	CPU_SPI0_CLK	CPU_SPI0_CLK	RB8	1	2	0	0201	5%	SPI_CLK
[11]	CPU_SPI0_SI	CPU_SPI0_SI	RB3	1	2	0	0201	5%	SPI_SI
[11]	CPU_SPI0_SO	CPU_SPI0_SO	RB6	1	2	0	0201	5%	SPI_SO
[11]	CPU_SPI0_IO2	CPU_SPI0_IO2	RB4	1	2	0	0201	5%	SPI_IO2
[11]	CPU_SPI0_IO3	CPU_SPI0_IO3	RB5	1	2	0	0201	5%	SPI_IO3



[27,79]	EC_SPI_CS0_N		EC_SPI_CS0_N	RB13	1		2	0	0201	5%	SPI_CS0_N	
[79]	EC_SPI_CLK		EC_SPI_CLK	RB10	1		2	1/20W	100	1%	0201	SPI_CLK
[79]	EC_SPI_SI		EC_SPI_SI	RB11	1		2	1/20W	100	1%	0201	SPI_SI
[79]	EC_SPI_SO		EC_SPI_SO	RB12	1		2	1/20W	100	1%	0201	SPI_SO

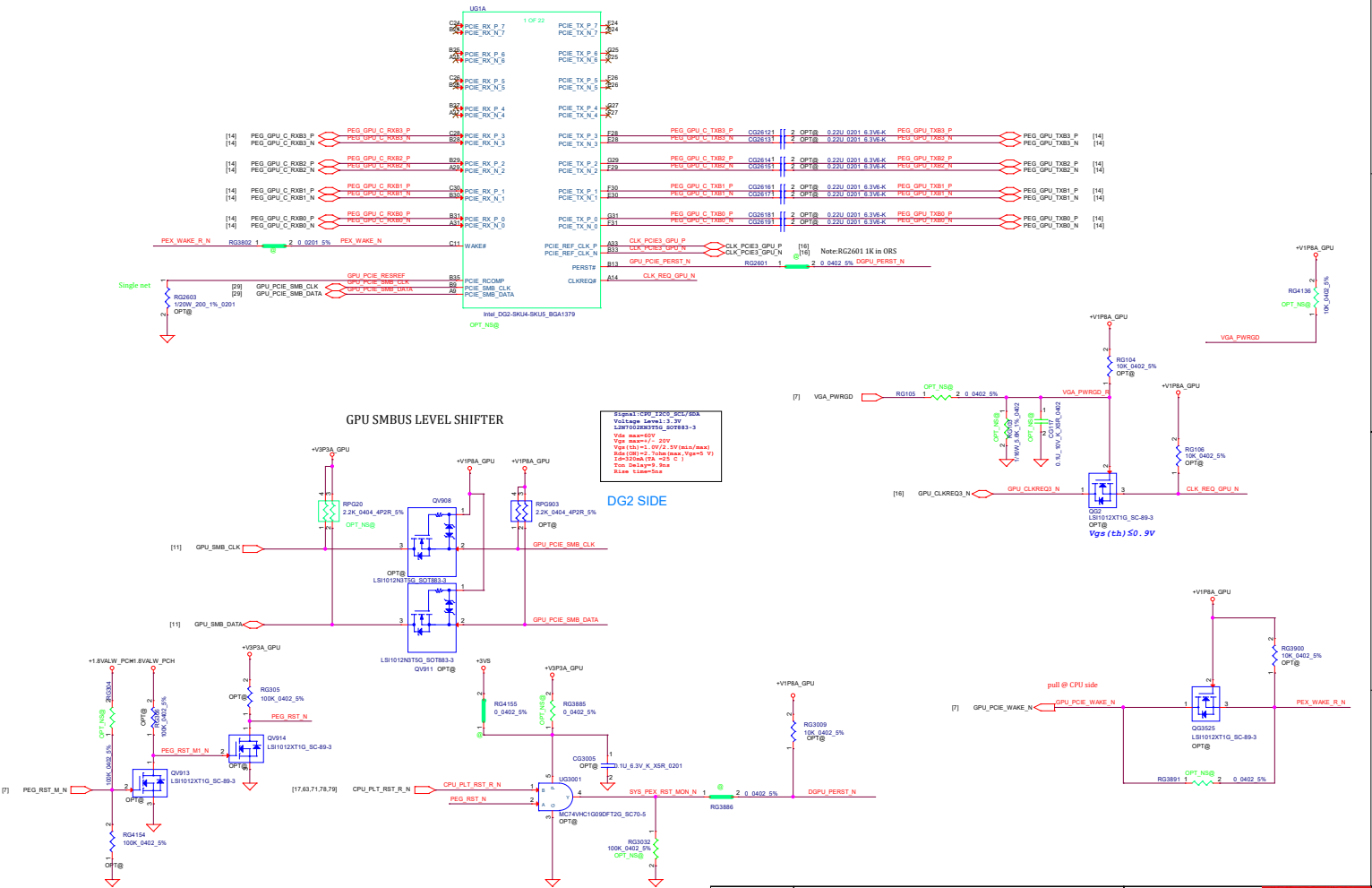
[27,79]	EC_SPI_CS0_N	RB25	1	2	0	0201	5%	
[11]	CPU_SPI0_CS1_N	RB9	1	2	0	0201	5%	SPI_CS1_N



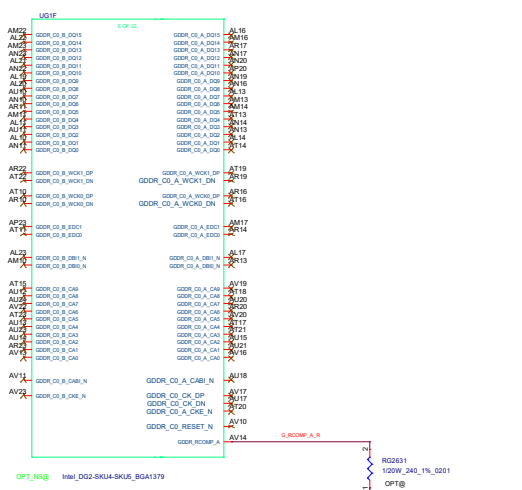
UB2 UB3 are changed FROM IQ to IN by common pool

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Issued Date		2012/07/01		Deciphered Date		2014/07/01		Size		Document Number	
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										0.1	
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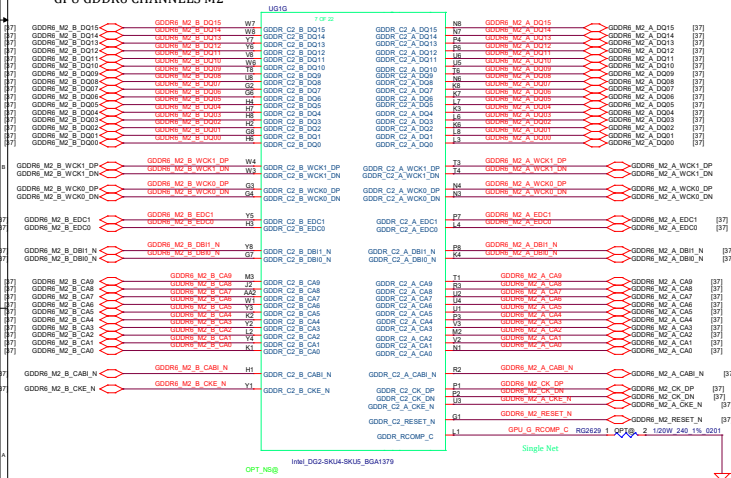
PCIE INTERFACE X4



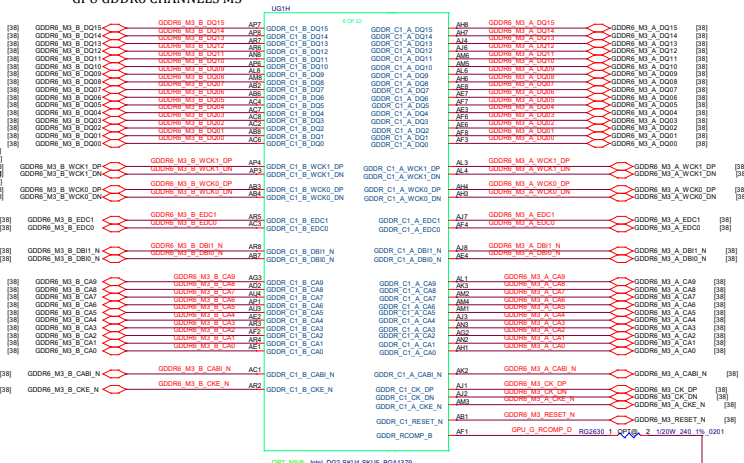
GPU GDDR6 CHANNELS M1



GPU GDDR6 CHANNELS M2



GPU GDDR6 CHANNELS M3

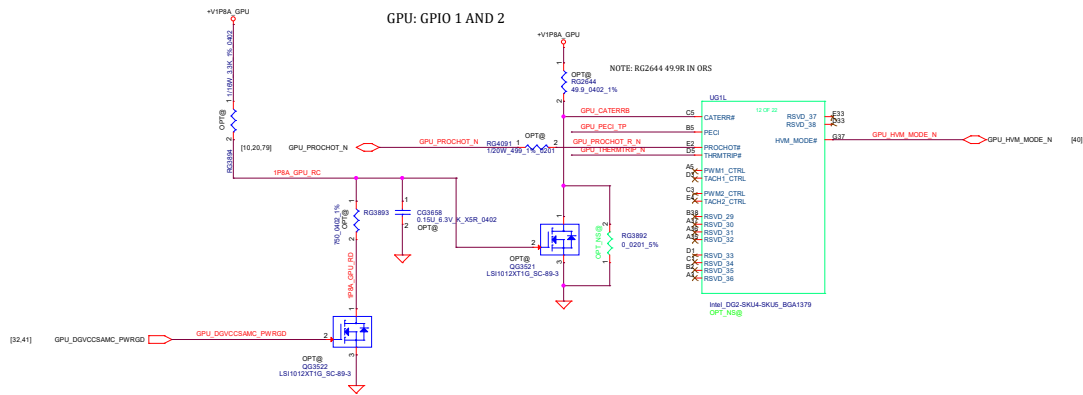


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Issued Date	2012/07/01	Deciphered Date
	2014/07/01	

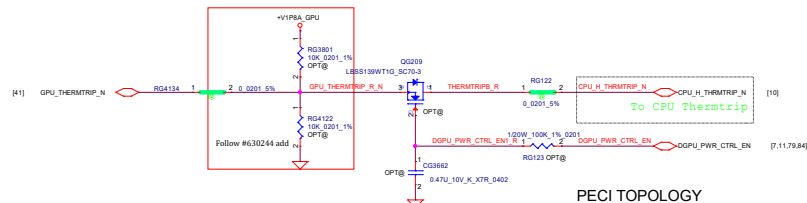
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Title		S170S370-IAL		LCFC	
Size	Document Number				
	P030-GPU MEM Interface (A/B)				
Date	2013, February 18, 2022	Issue	30	13	

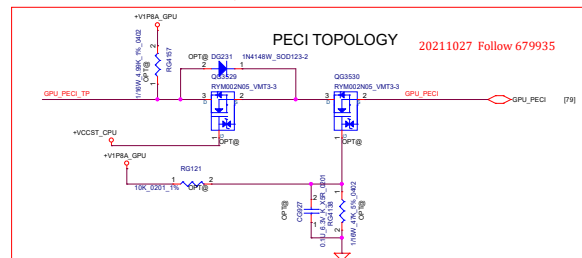
GPU: GPIO 1 AND 2



NEW ADD FOLLOW 630244



PECI TOPOLOGY



EMC/RF Required

GPU_THERMTRIP_R_N CG15 1 2.1U 6.3V K X5R 0201
GPU_PROCHOT_R_N CG16 1 2.1U 6.3V K X5R 0201

EMC REQUIRED 0624

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Issued Date	2021/01/19	Deciphered Date	2022/01/19

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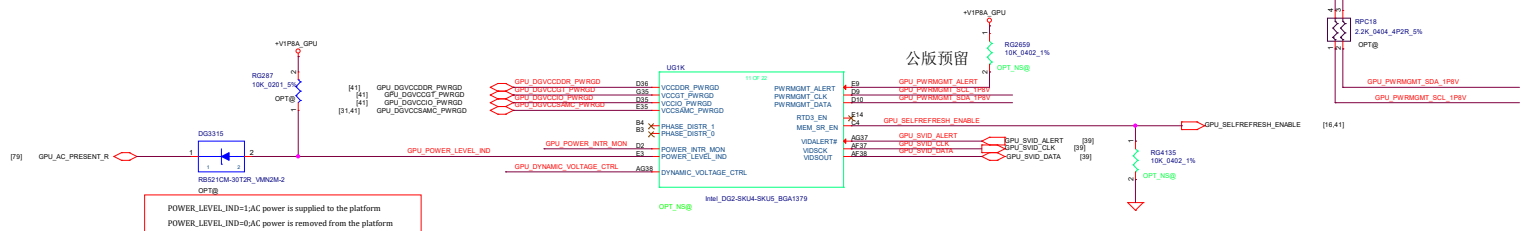
Title	S170/S370-IAL
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Size C	Document Number P031-
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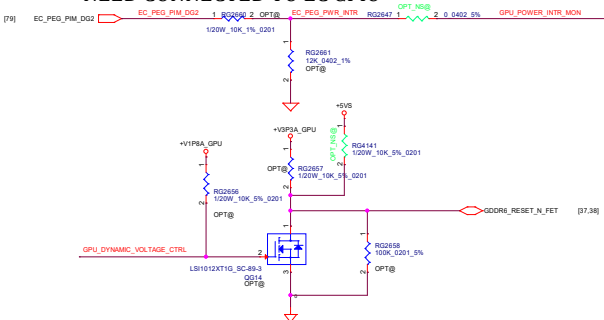
Date: Friday, February 18, 2022 Sheet 31 of 113

LCFC

GPU: GPIO 1 AND 2



NEED CONNECTED TO EC GPIO



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Issued Date	2012/07/01	Deciphered Date	2014/07/01		<div style="background-color: red; color: white; padding: 5px; text-align: center; font-weight: bold;">LCFC</div>
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Size	Document Number		Rev		
	P032-GPU G20/JTAG		1		
Date	C996-CPU C992		32	of 113	

GPU: DEBUG & RSVD

DEBUG

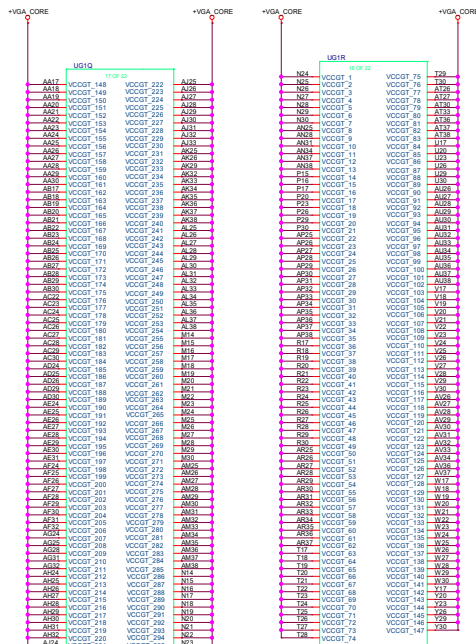
RSVD

GPU DDI: A,C,D

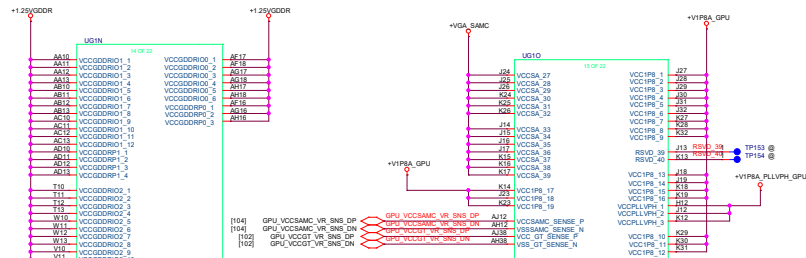
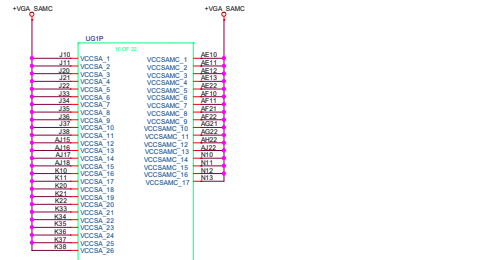
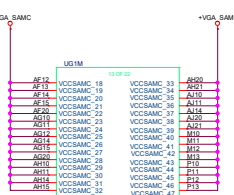
GPU DDI:B

BOARD IDENTIFICATION FOR DG2 FIRMWARE

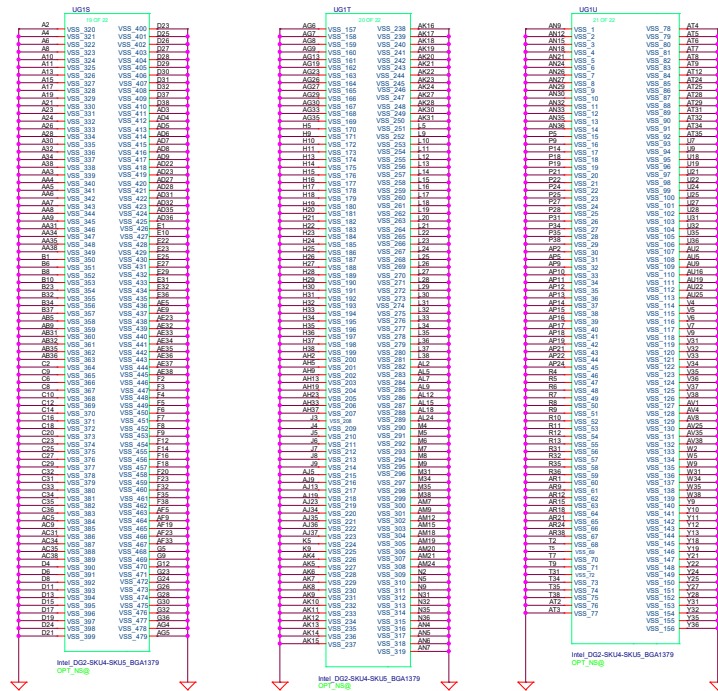
GPU POWER: VCCGT



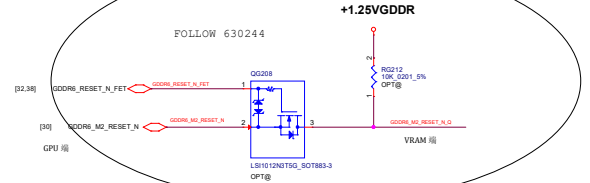
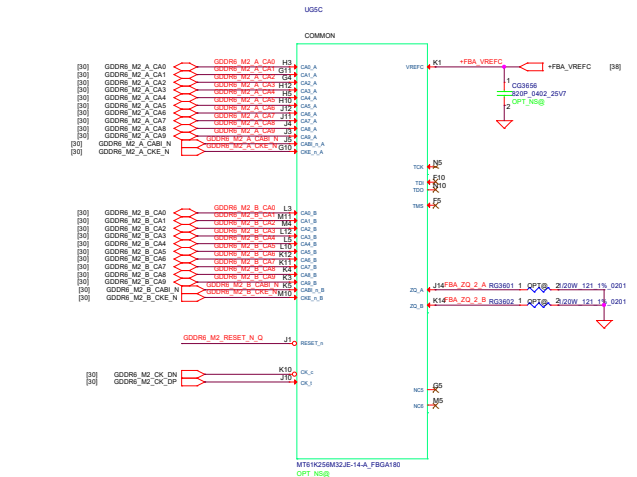
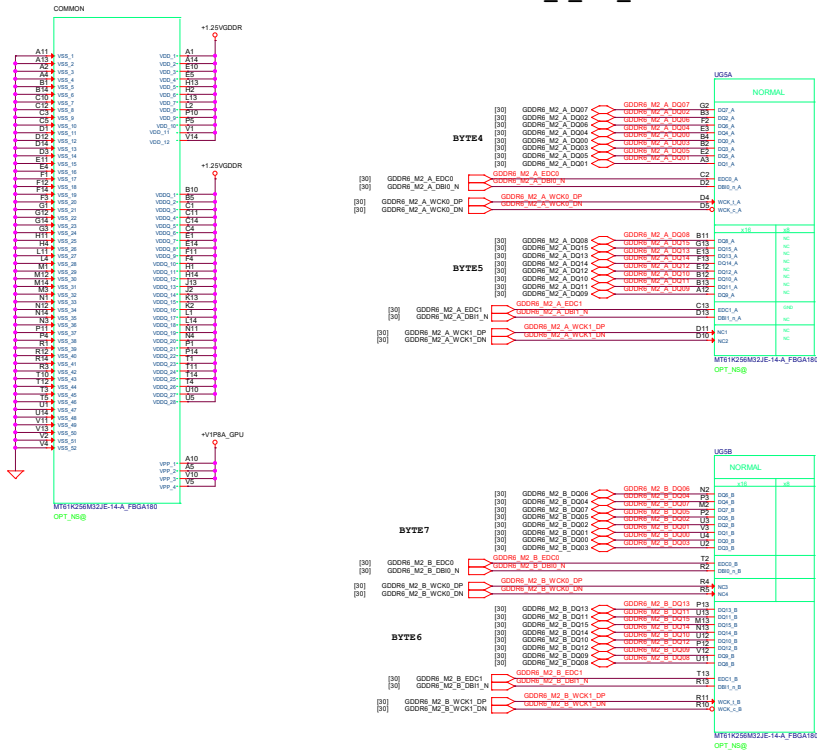
GPU POWER: OTHER



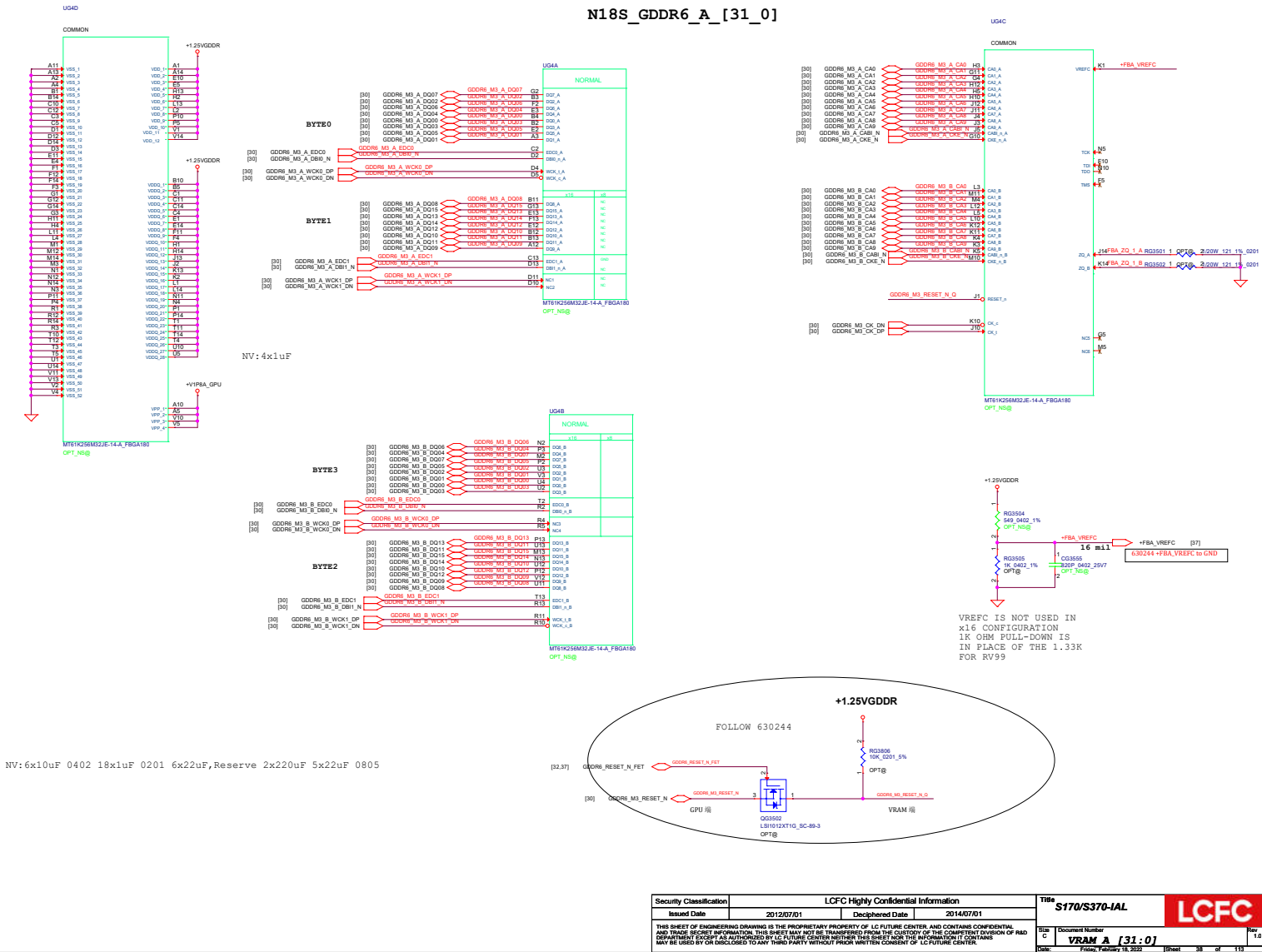
GPU POWER: GROUND



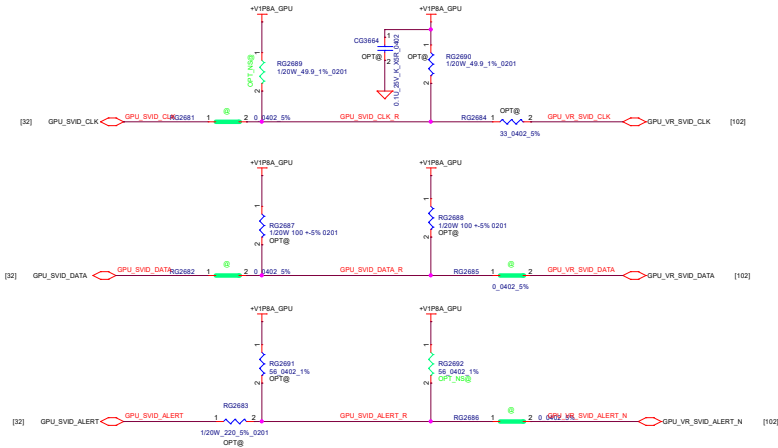
GDDR6_A [63_32]

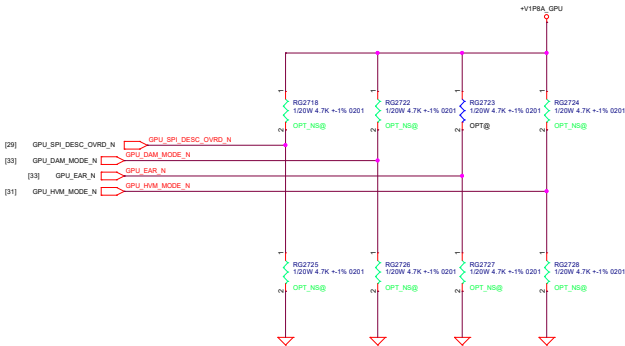


N18S_GDDR6_A [31_0]

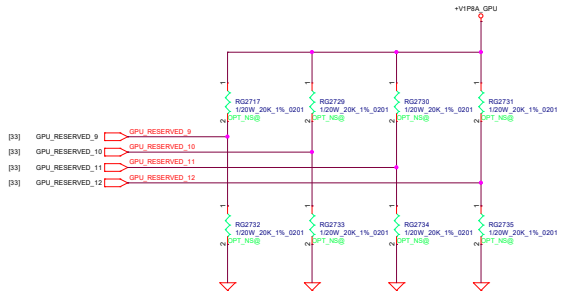


GPU VREG: SVID



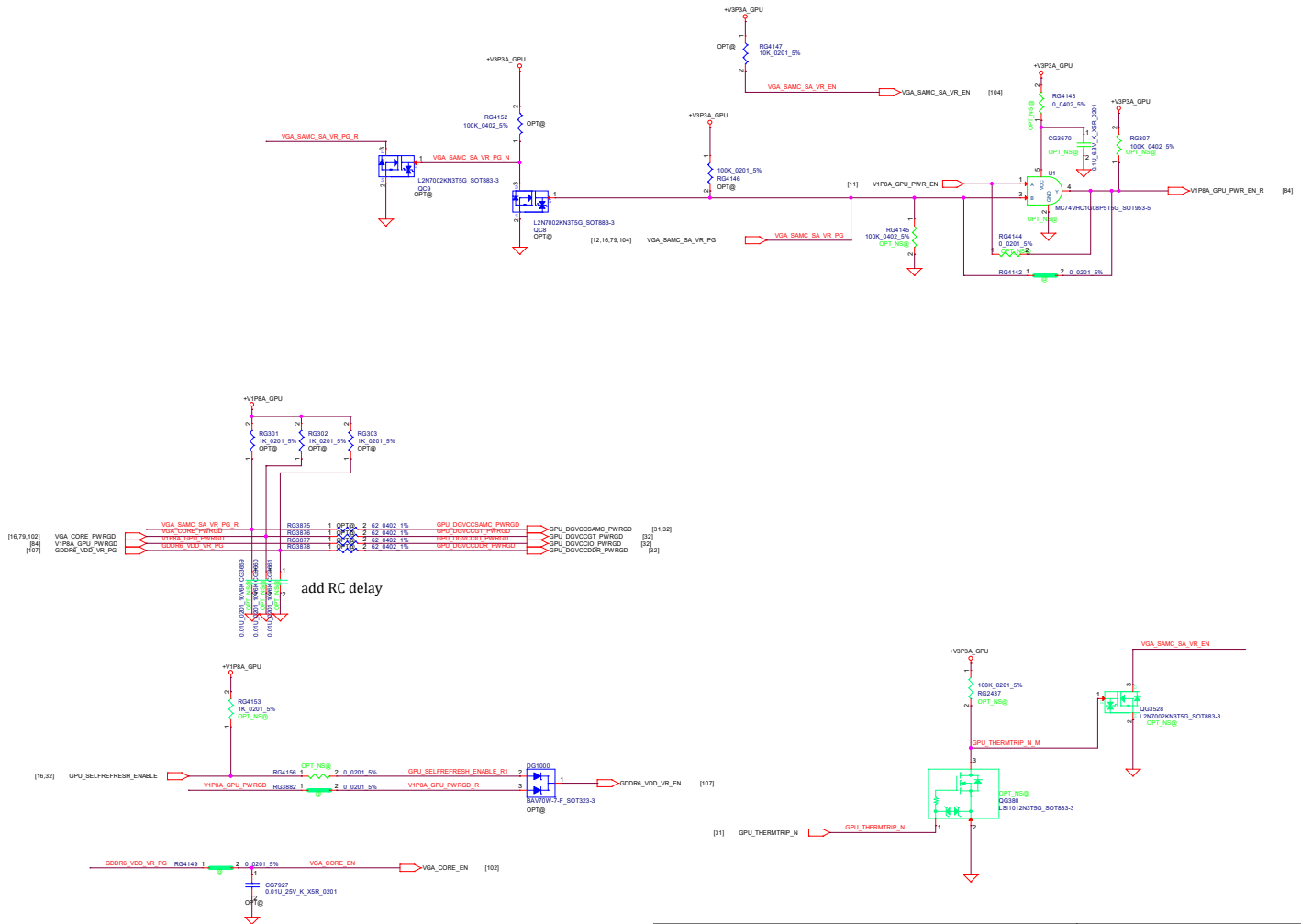


- [29] GPU_SPL_DESC_OVRD_N → GPU_SPL_DESC_OVRD_N
- [30] GPU_DAM_MODE_N → GPU_DAM_MODE_N
- [33] GPU_EAR_N → GPU_EAR_N
- [31] GPU_HVM_MODE_N → GPU_HVM_MODE_N



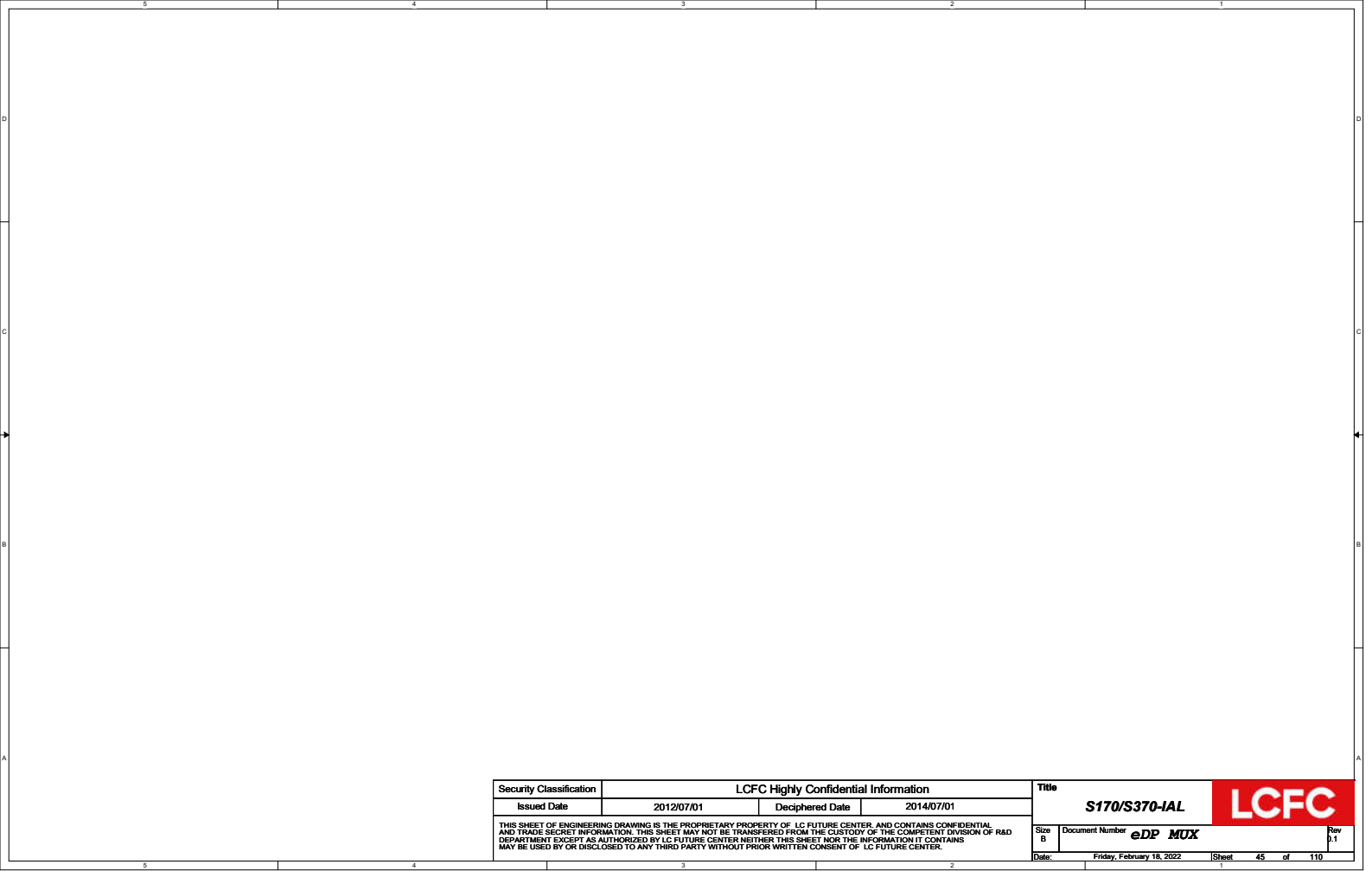
- [33] GPU_RESERVED_9 → GPU_RESERVED_9
- [33] GPU_RESERVED_10 → GPU_RESERVED_10
- [33] GPU_RESERVED_11 → GPU_RESERVED_11
- [33] GPU_RESERVED_12 → GPU_RESERVED_12

GPU POWER SEQUENCING

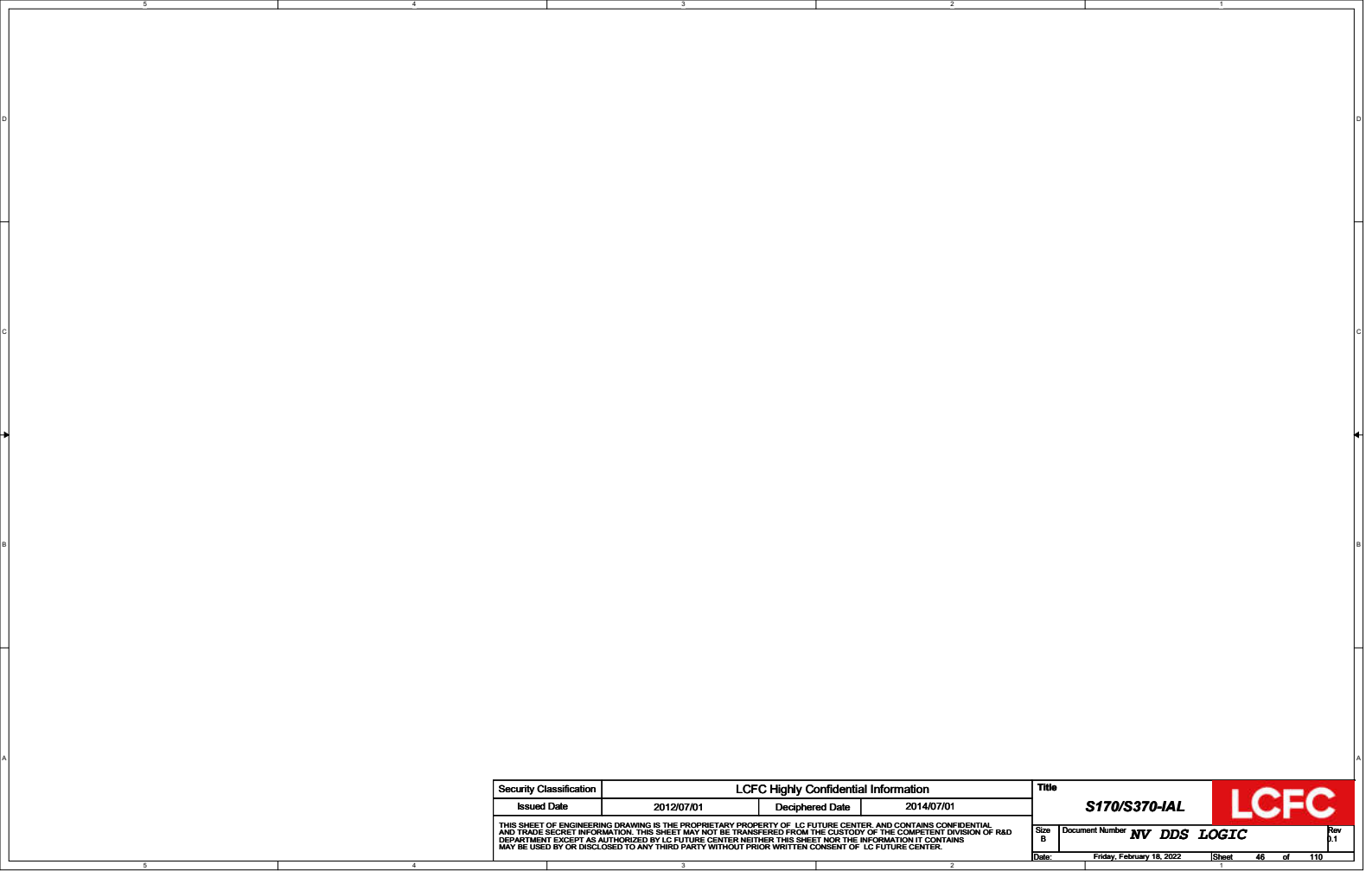



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Doc No	P041-VRAN C [31.0] -NA	Doc Number	[31.0]	Rev
Date	1986/01/01	Issue	41	1.0

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Size		C		Document Number		P042-VRAM C [64:32]--NA		Rev 1.0	
Date:		Friday, February 18, 2022		Sheet		48		of 115	

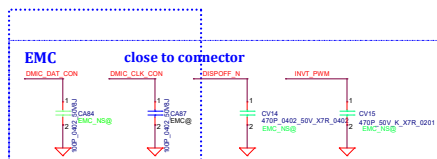
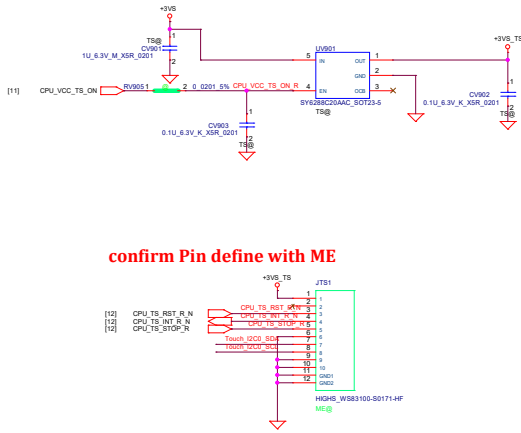


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				Date: Friday, February 18, 2022	
				Sheet 45 of 110	Rev 0.1

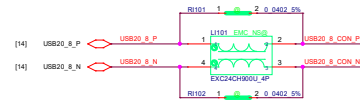
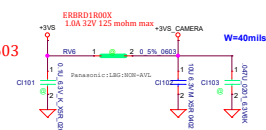


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Size B	Document Number NV DDS LOGIC			Rev 0.1	
Date:		Friday, February 18, 2022		Sheet 46 of 110	

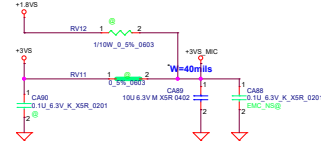
1.C970EDP connector pindefine different with S370&V14V15

[illegible]

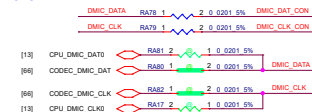
FI101 CHANGE TO 00HM 0603



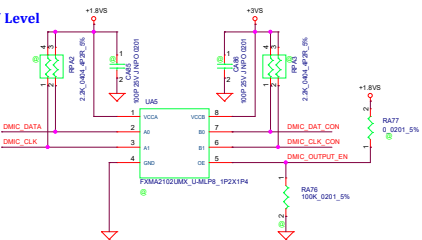
FA1 FA2 CHANGE TO 00HM 0603




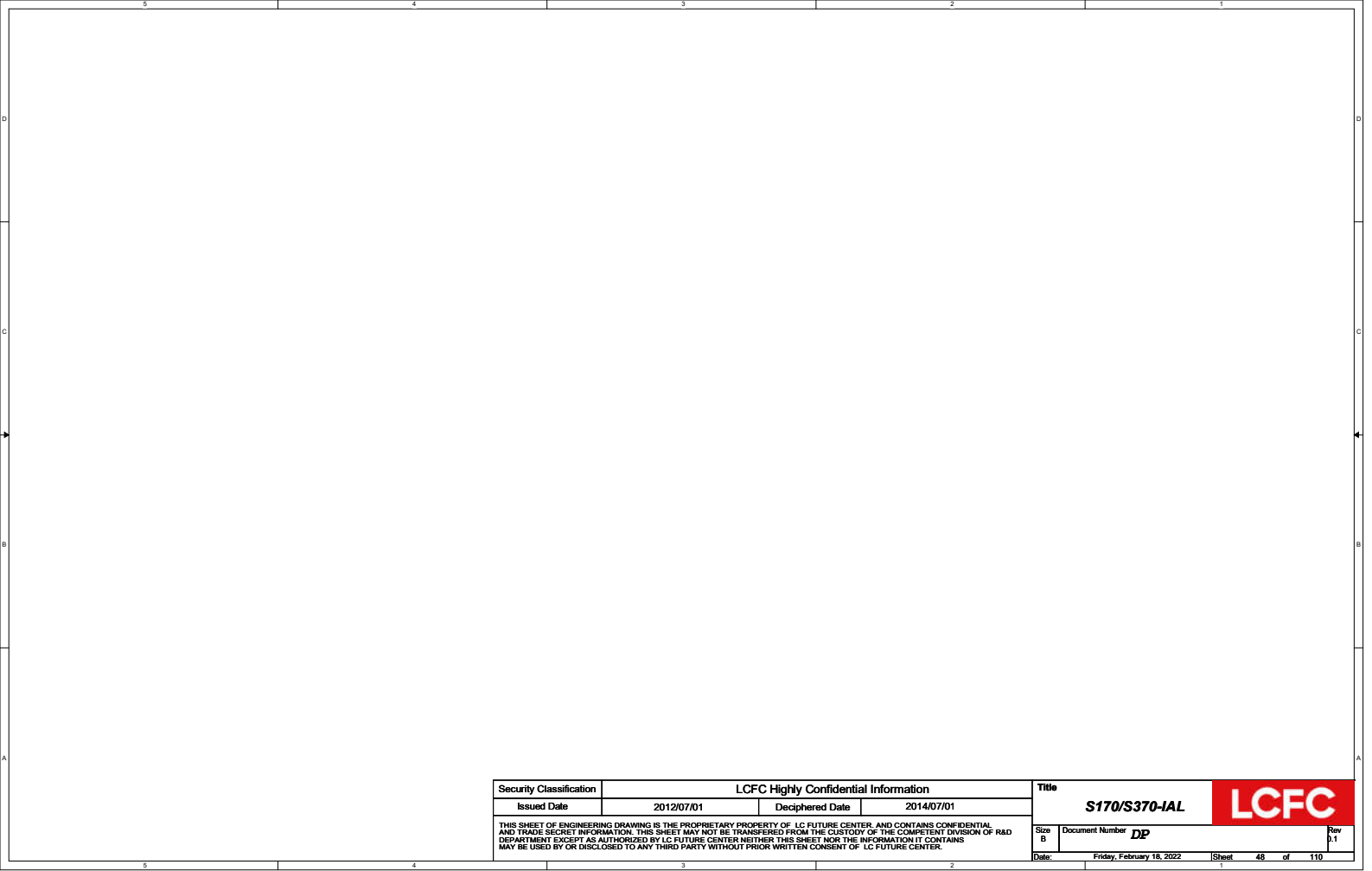
DMIC 3.3V Level



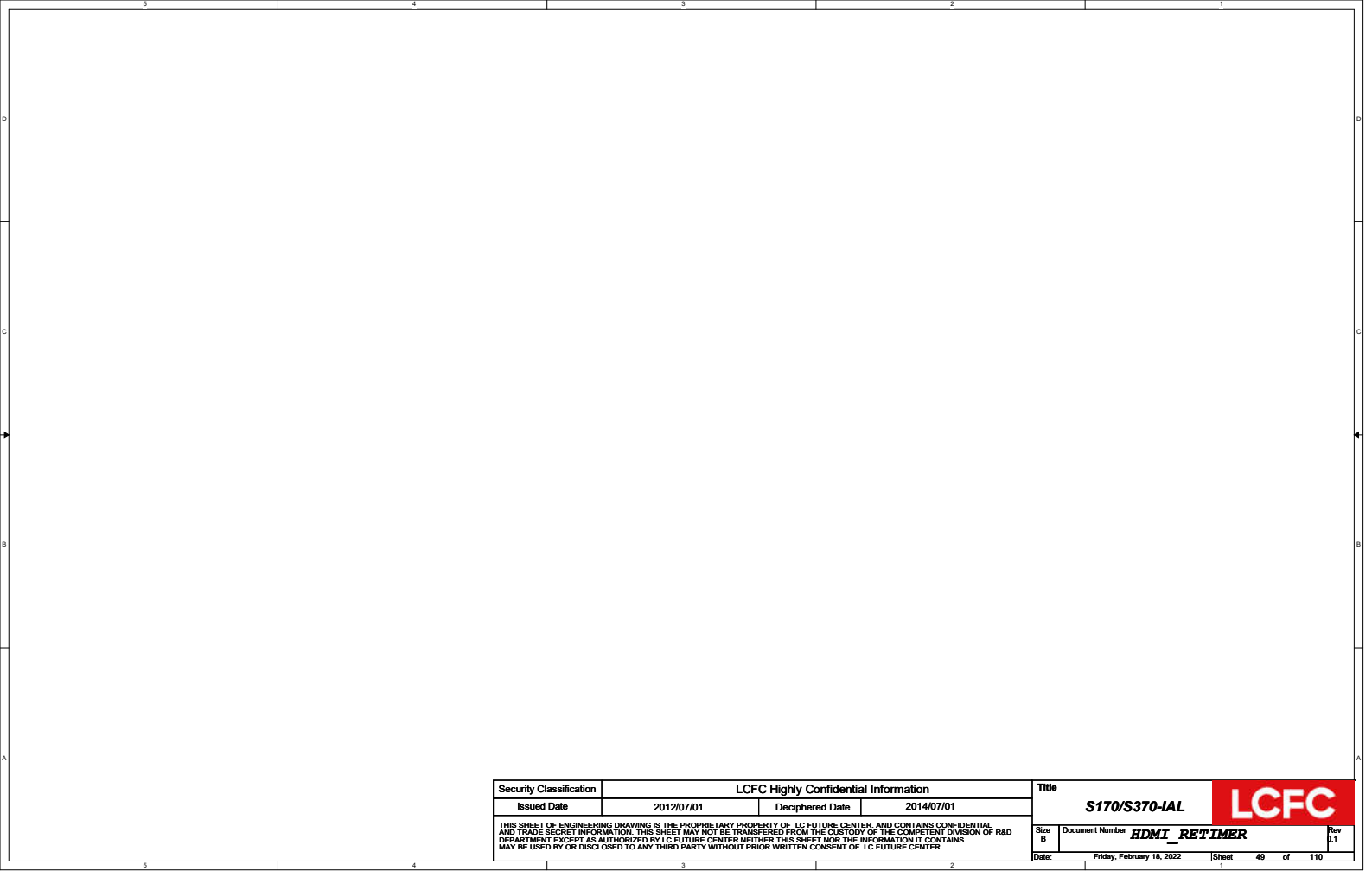
DMIC 1.8V Level



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Scale	Friday, February 18, 2022			Sheet			47 of 150		



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					Document Number DP
					Rev 0.1
Date: Friday, February 18, 2022					Sheet 48 of 110

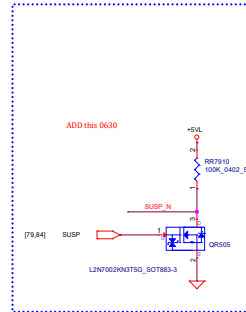


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				HDMI_RETIMER	
				Date:	Friday, February 18, 2022
				Sheet	49 of 110



Rev
0.1

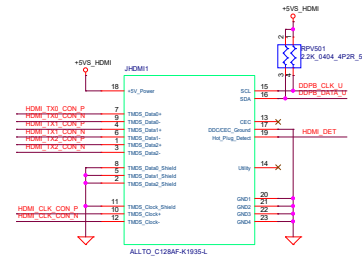
HDMI Power



the diffrent with Base:
1.C970 No HDMI CONN,S170 have

EMC

RV515 518 521 524 STUFF 300 FOLLOW S360?



MEQ
Conector list USE C128AF-K1939-L.Gold Plating diffrent


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			Date	Friday, February 18, 2022	Sheet	50 of 116

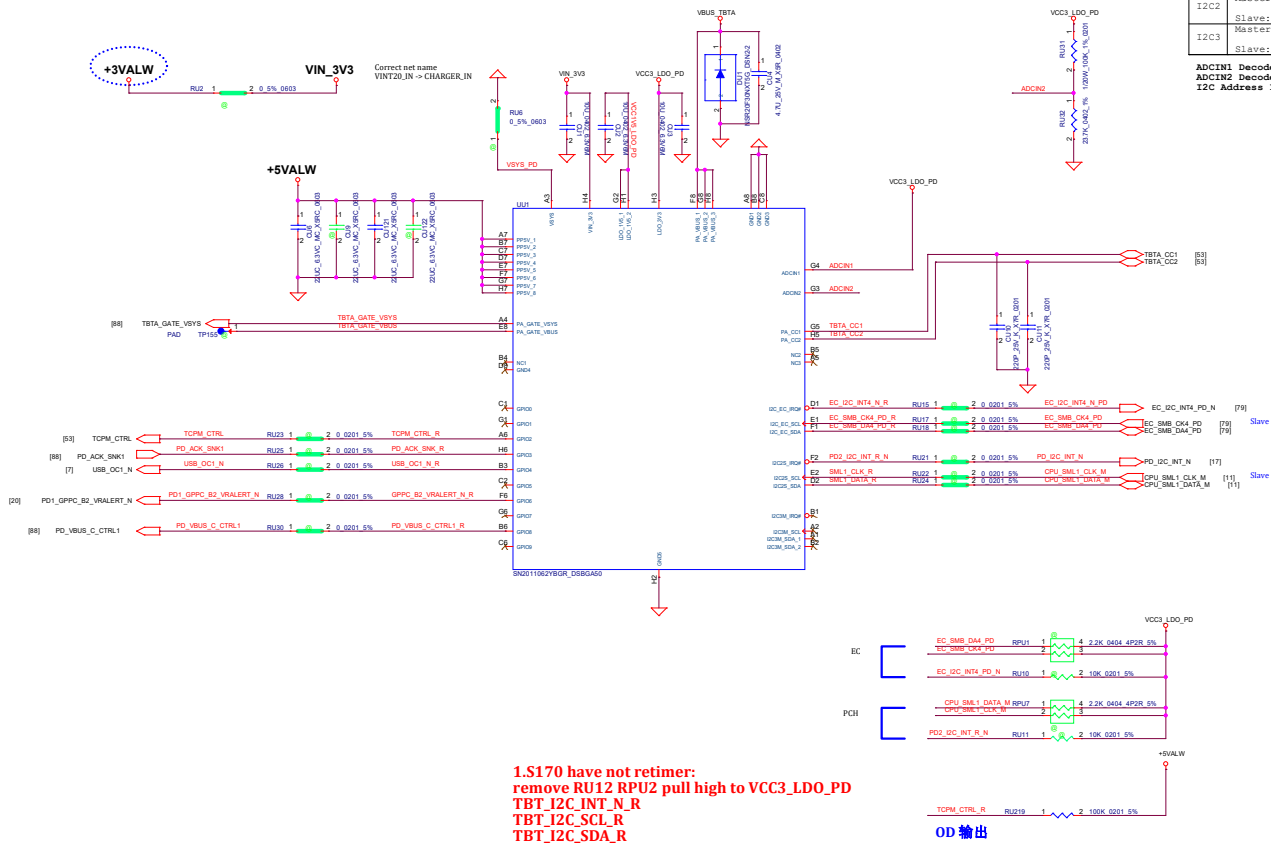
TABLE I2C Addressing

I2C1	Master: EC	TBTA PORT 0x20
	Slave: PD	
I2C2	Master: PMC	TBTA PORT 0x20
	Slave: PD	
I2C3	Master: PD	TBTA PORT 0.B.D.
	Slave: RT	

ADCIN1 Decoded: 7 --tie to LDO_3V3

ADCIN2 Decoded: 4 --0.3022

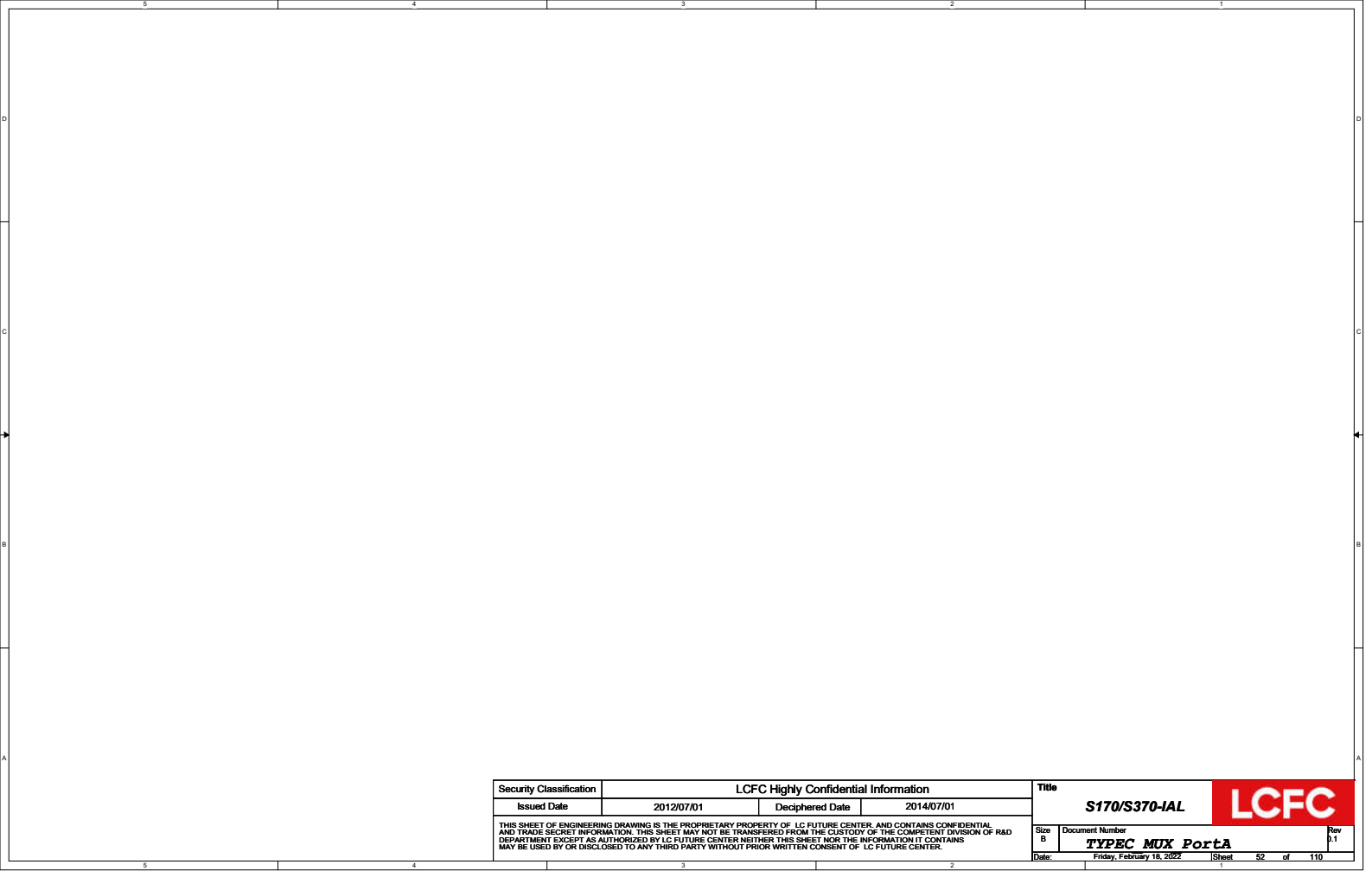
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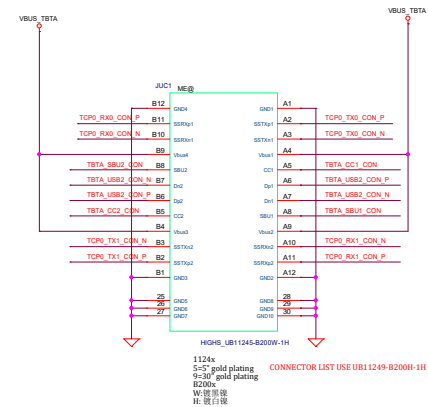
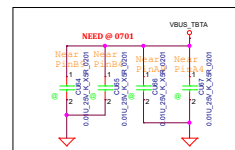
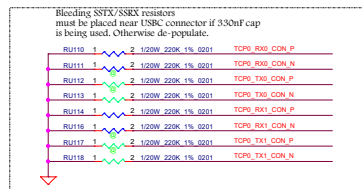
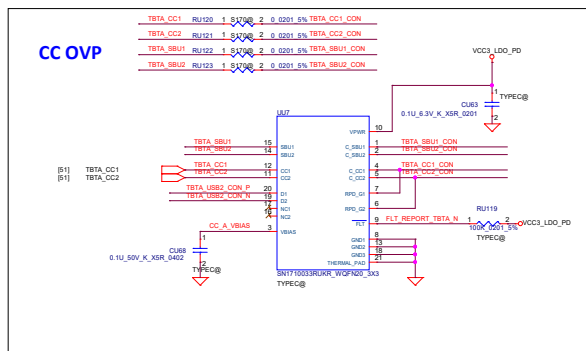
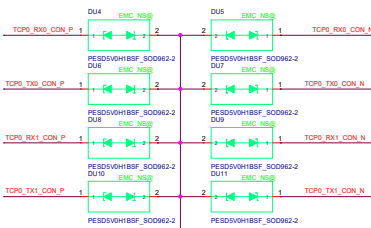
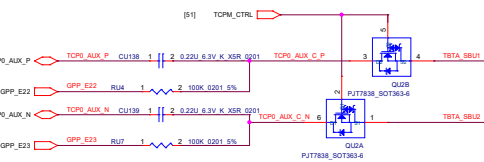
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Title		S170/S370-IAL		LCFC	
Size	Document Number	TYPEC Controller PortA		Rev	1.0
Date		Friday, February 18, 2022	18:00	51	of 110



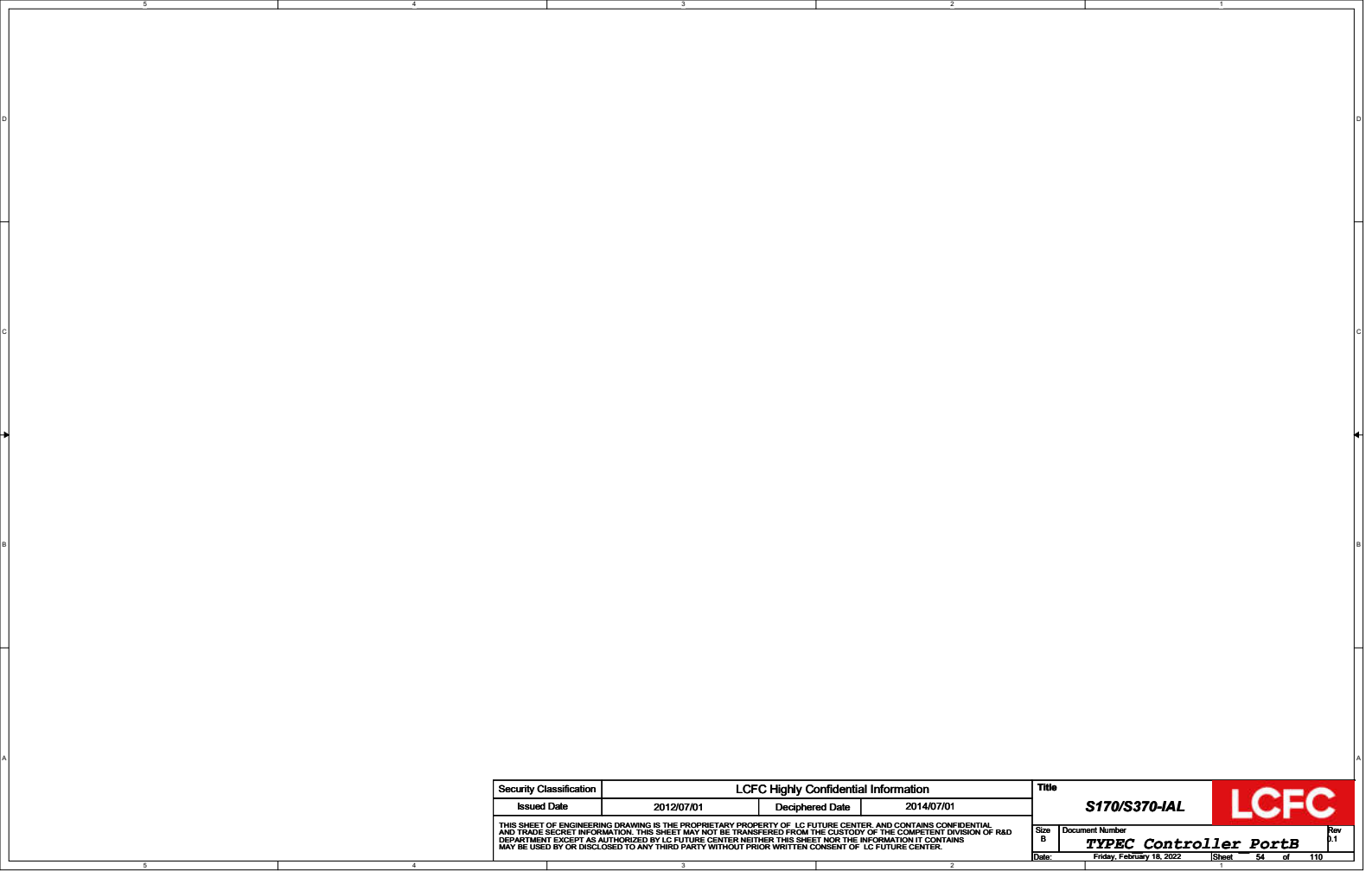
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Issued Date		2012/07/01	Deciphered Date	2014/07/01	S170/S370-IAL
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Size	Document Number				
B	TYPEC MUX Porta				Rev 0.1
Date:	Friday, February 18, 2022				Sheet 52 of 110



LCFC

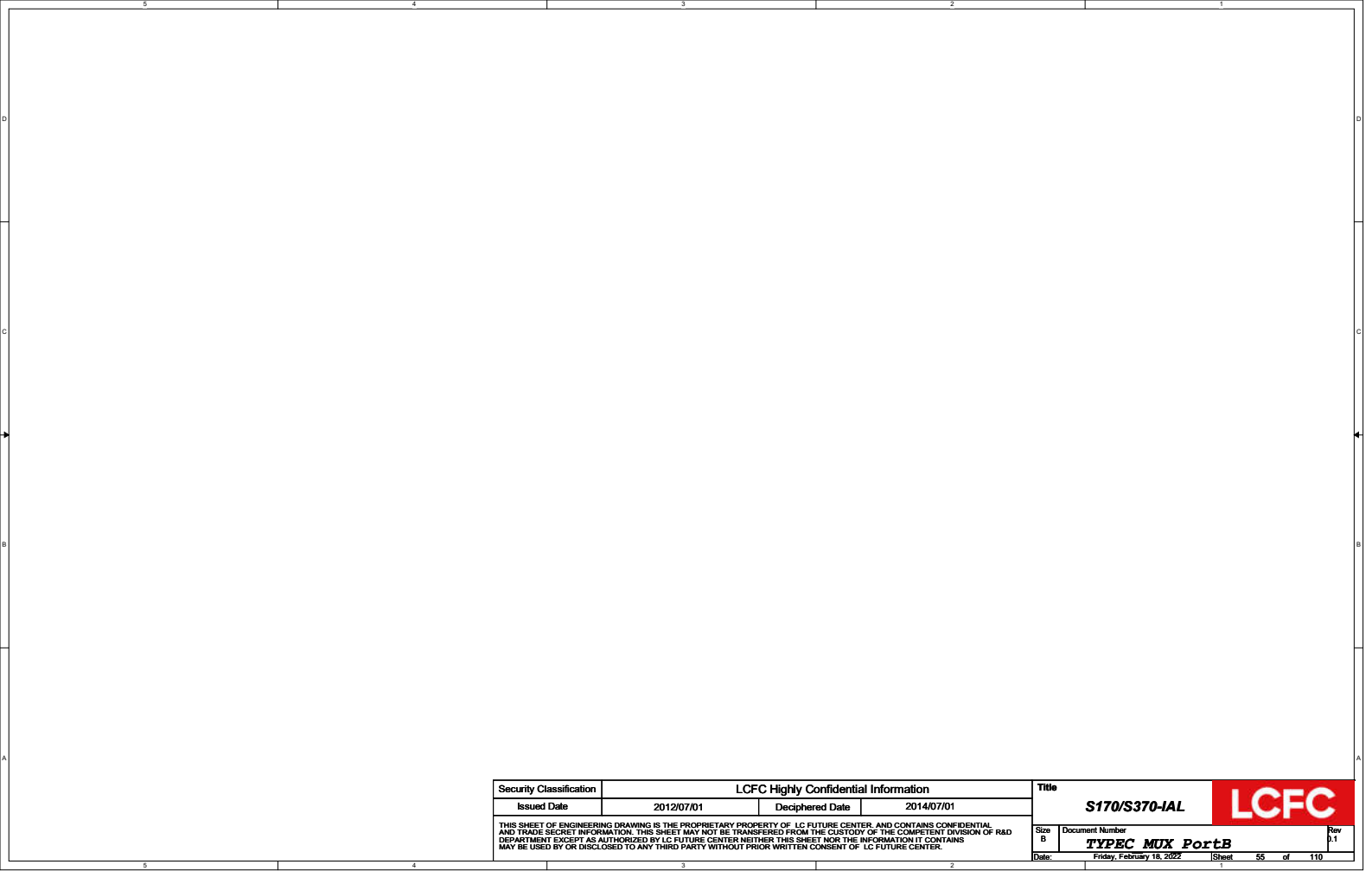
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Size C	Document Number TYPEC CONN Porta	Rev 1
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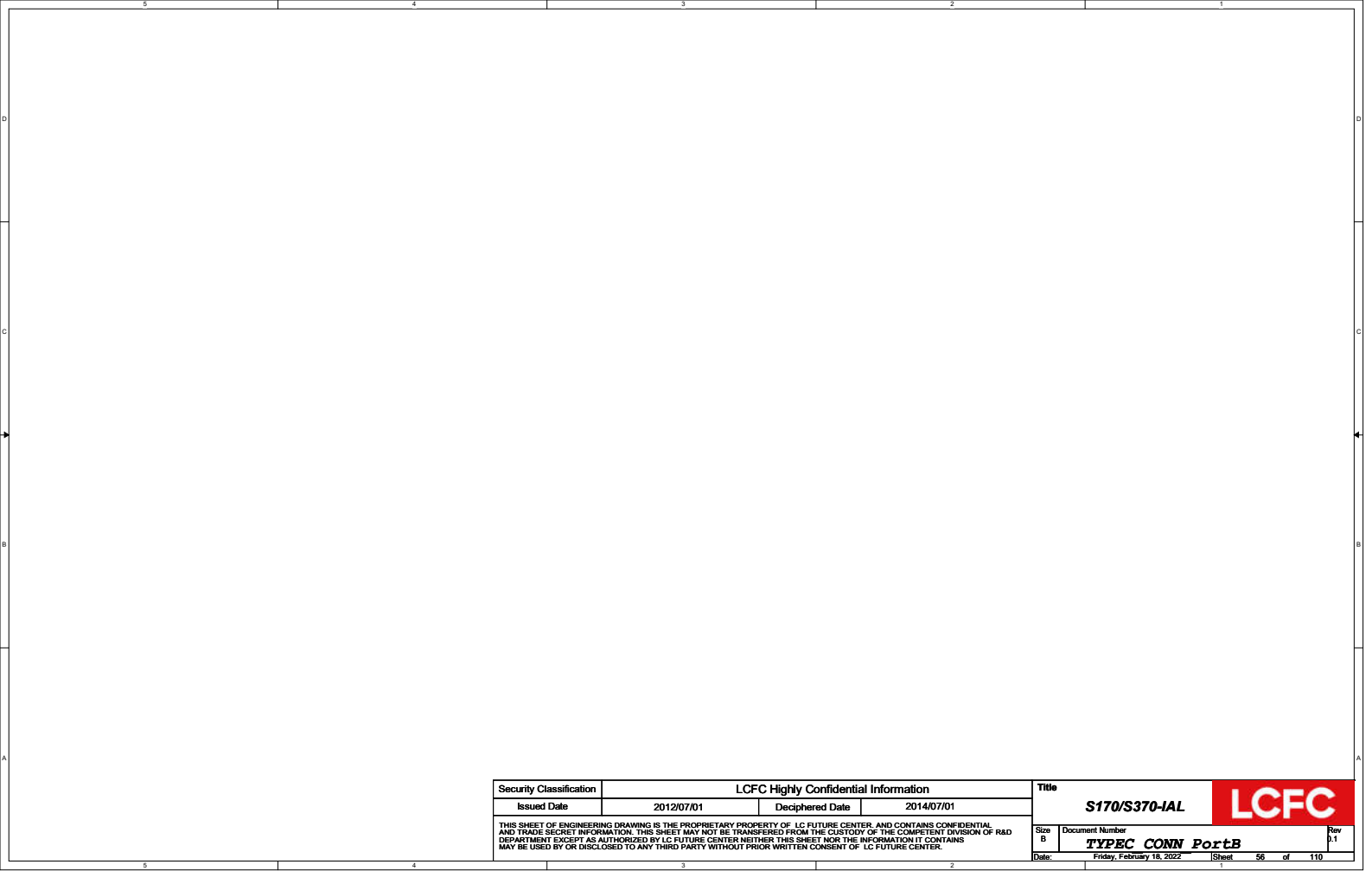


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				TYPEC Controller PortB	
Date:				Friday, February 18, 2022	Sheet 54 of 110





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				TYPEC MUX PortB	
Date:				Friday, February 18, 2022	1 Sheet 55 of 110
				Rev	0.1

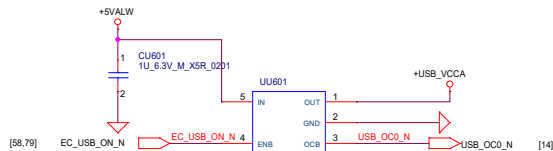


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				TYPEC CONN PortB	
Date:				Friday, February 18, 2022	1 Sheet 56 of 110

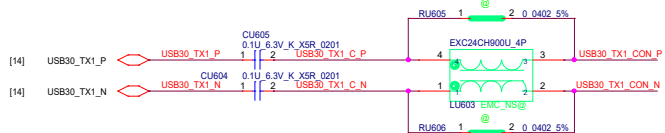
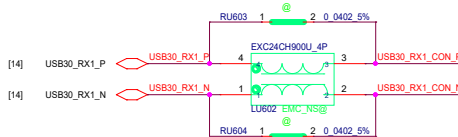
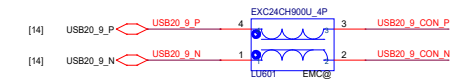
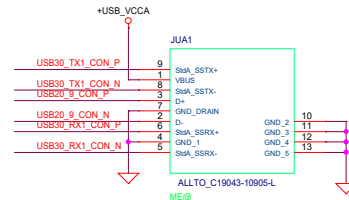
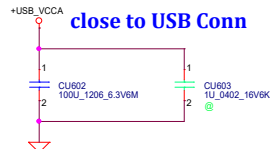


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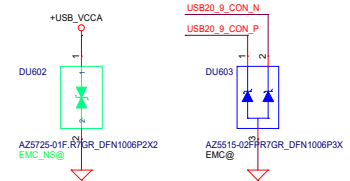
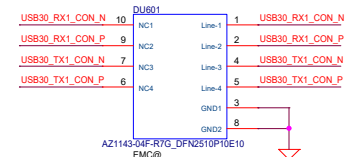
USB3.0 PORT



Low Active 2A



EMC close to USB Conn



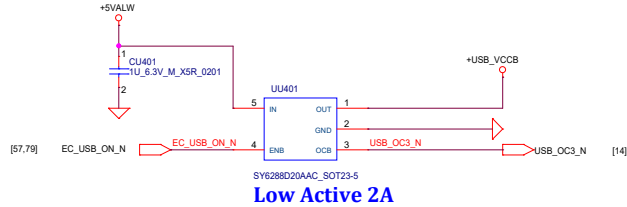
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				USBA PortA	
				Date	Friday, February 18, 2022
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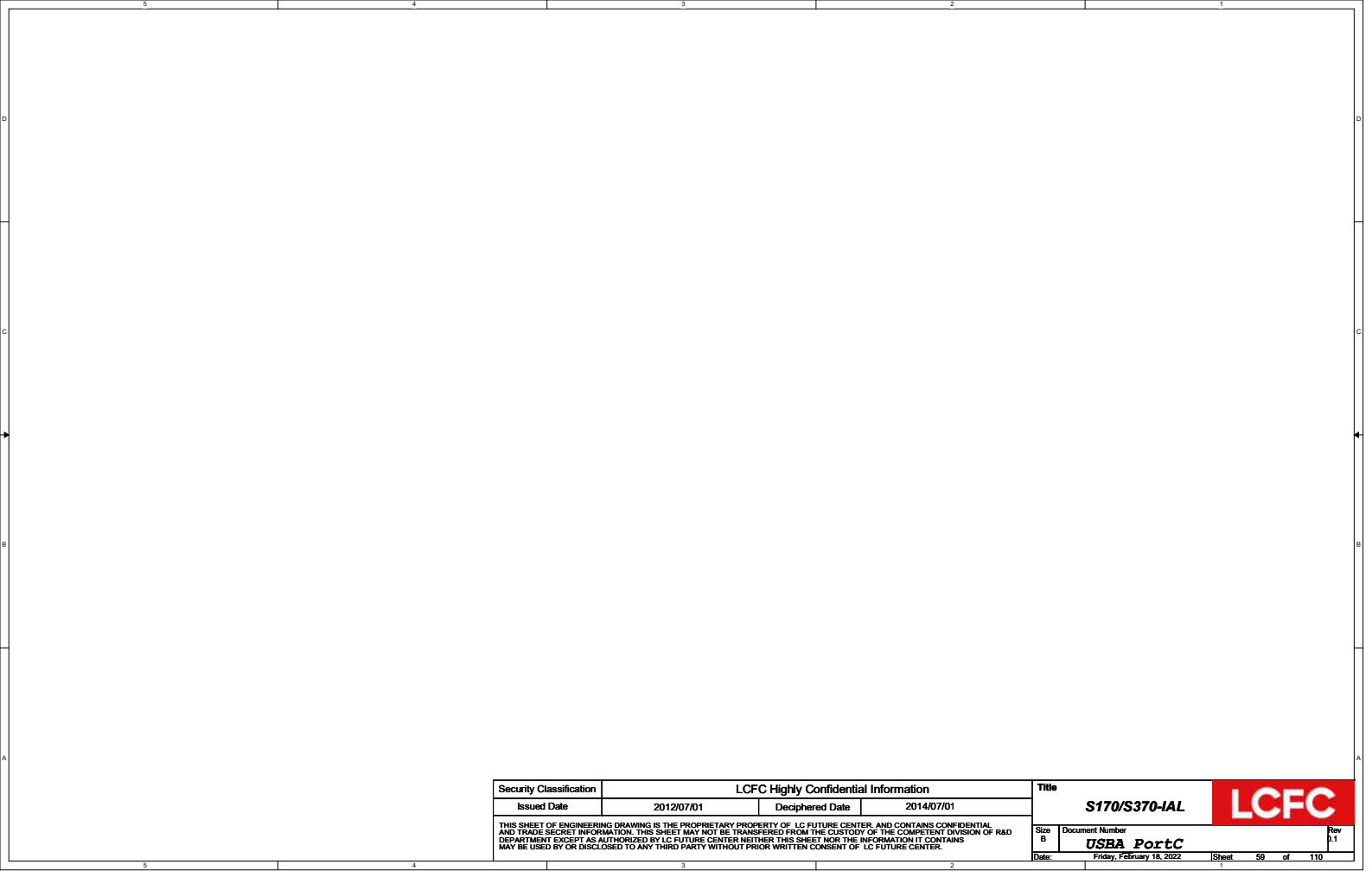
USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board

USB2.0 PORT

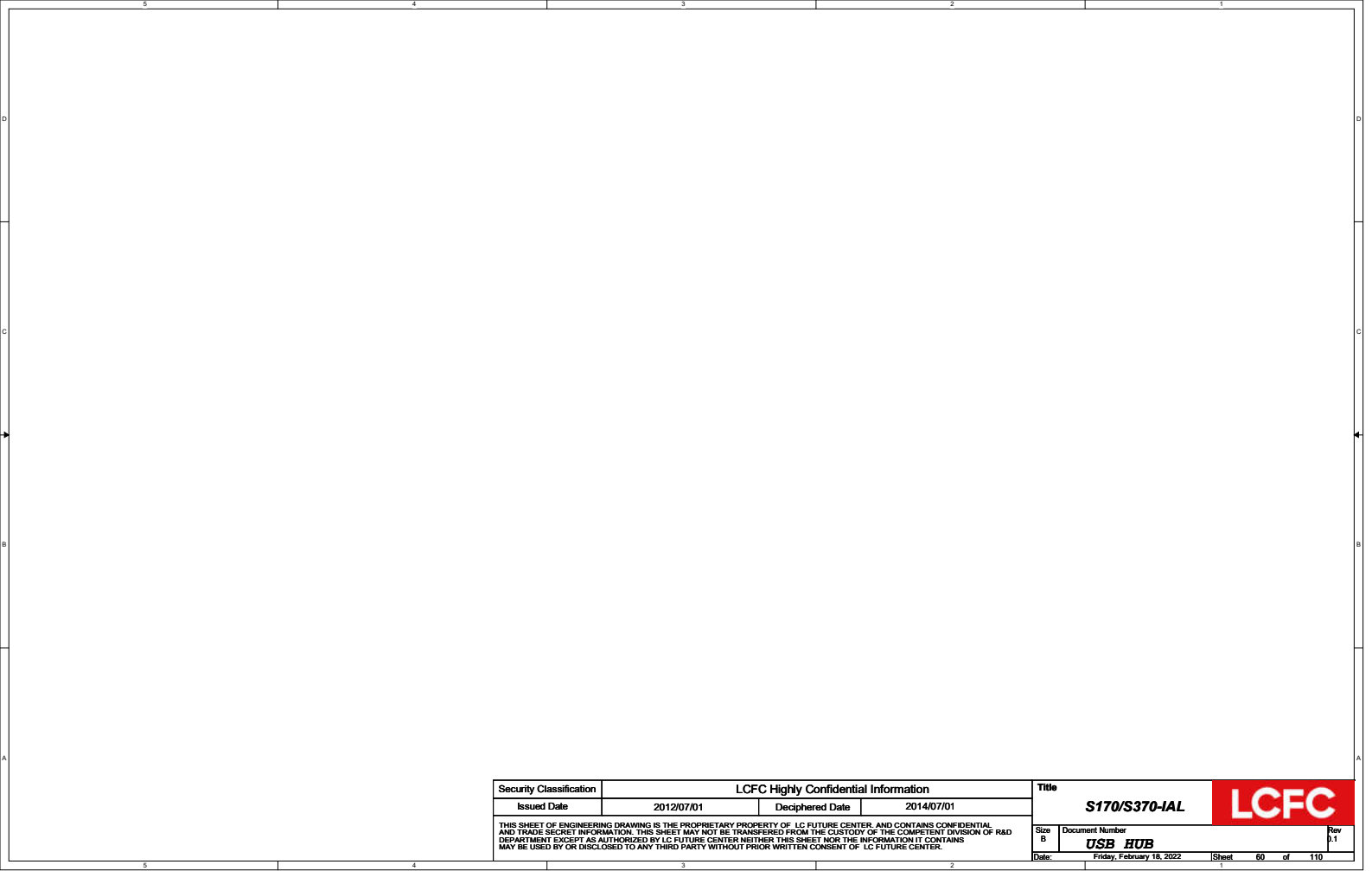


the diffrent with Base:
1.C970 No USB2.0 only,S360&V14V15 have

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				USBA PortB	Rev 0.1
				Date:	Friday, February 18, 2022
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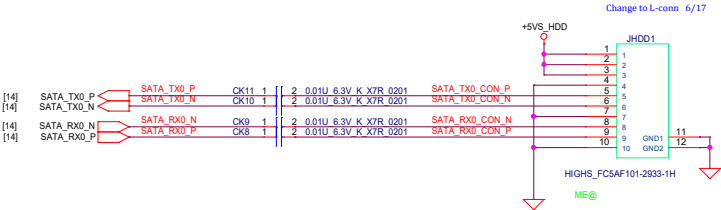
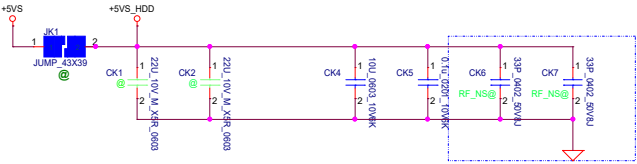
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Size B	Document Number USB HUB				Rev 0.1
Date:	Friday, February 18, 2022			Sheet 60	of 110

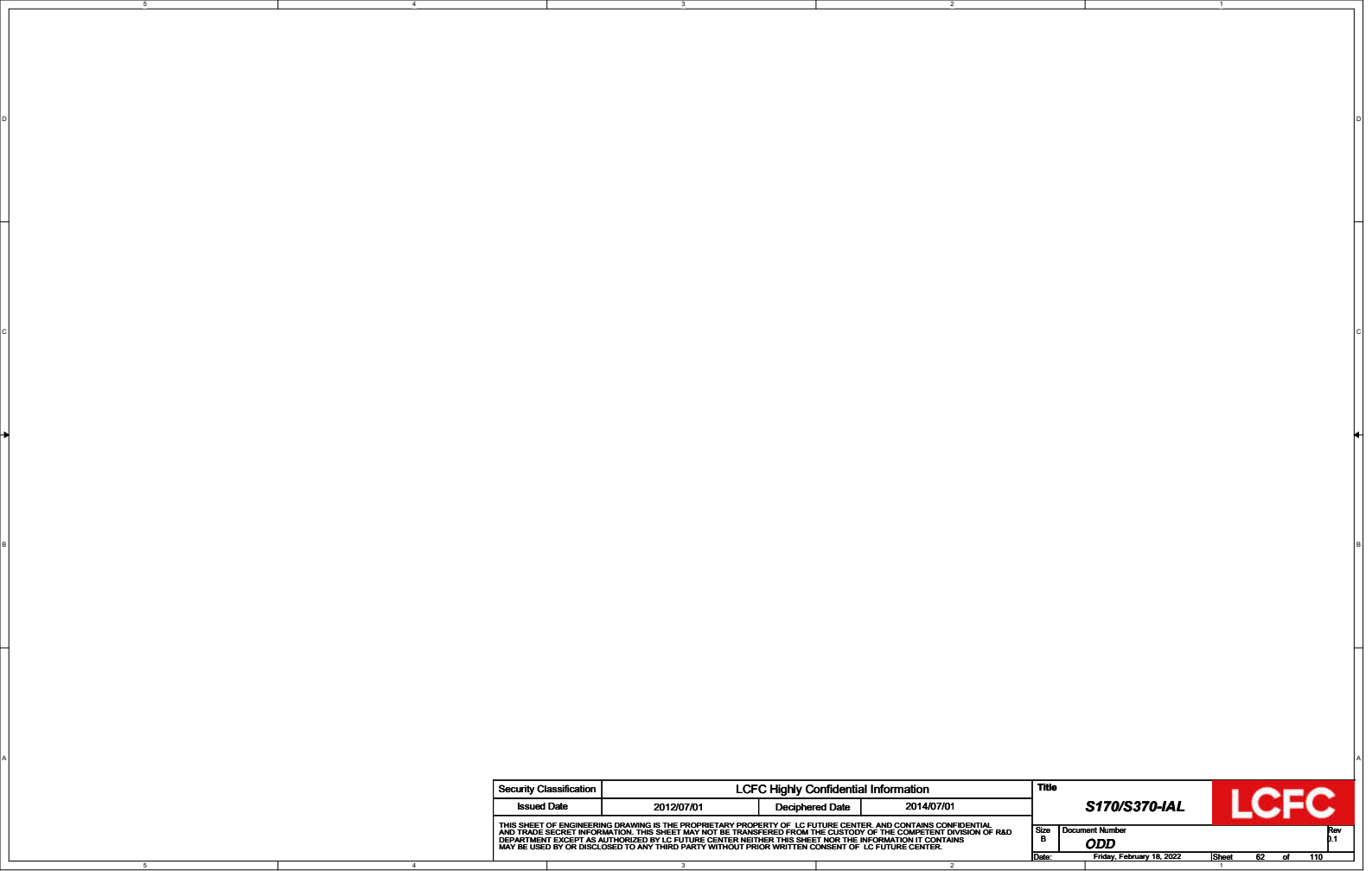


HDD Power



REXT: external res for output swing adjustment
it can be left open or tie to GND, internally generated bias
current be used and the output is as default swing setting;
the pin can be connected 4.99k to GND, the output swing
will be at the default value with Reference to the ex RES
DEW: De-emphasis width setting for A&B

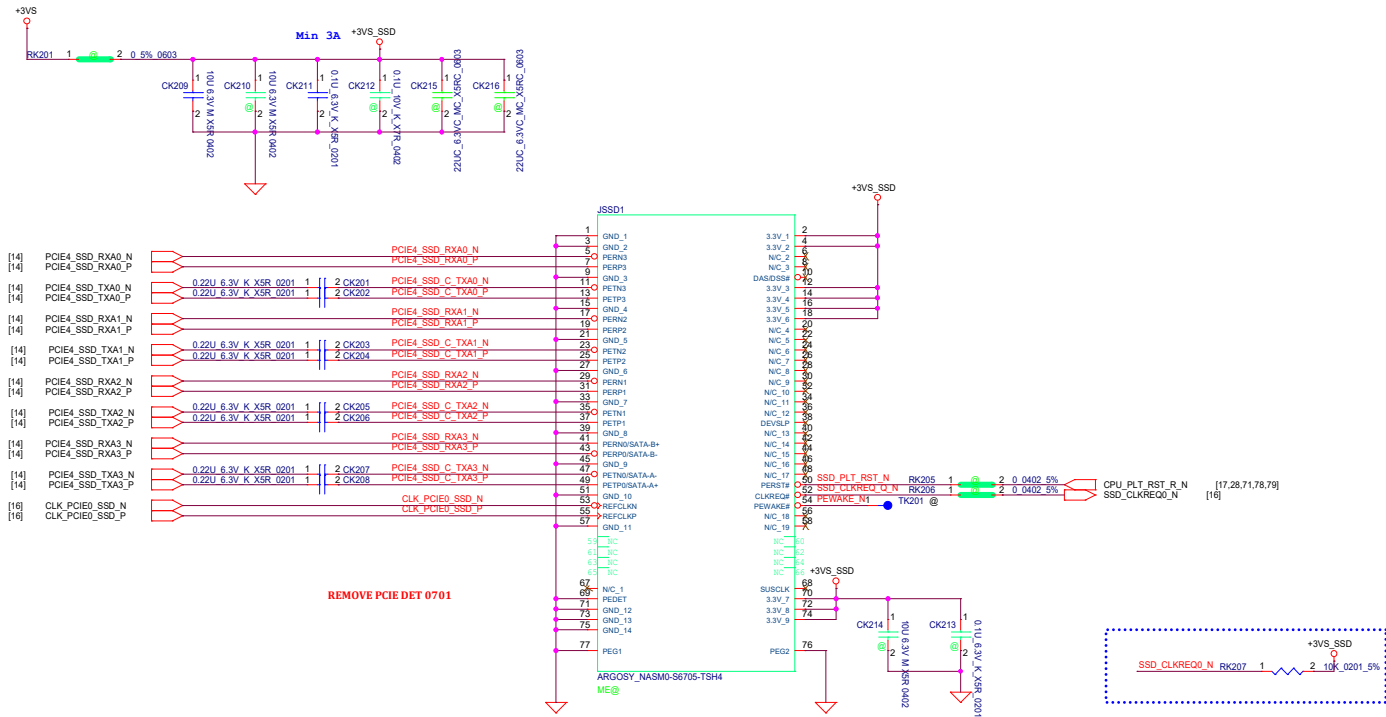
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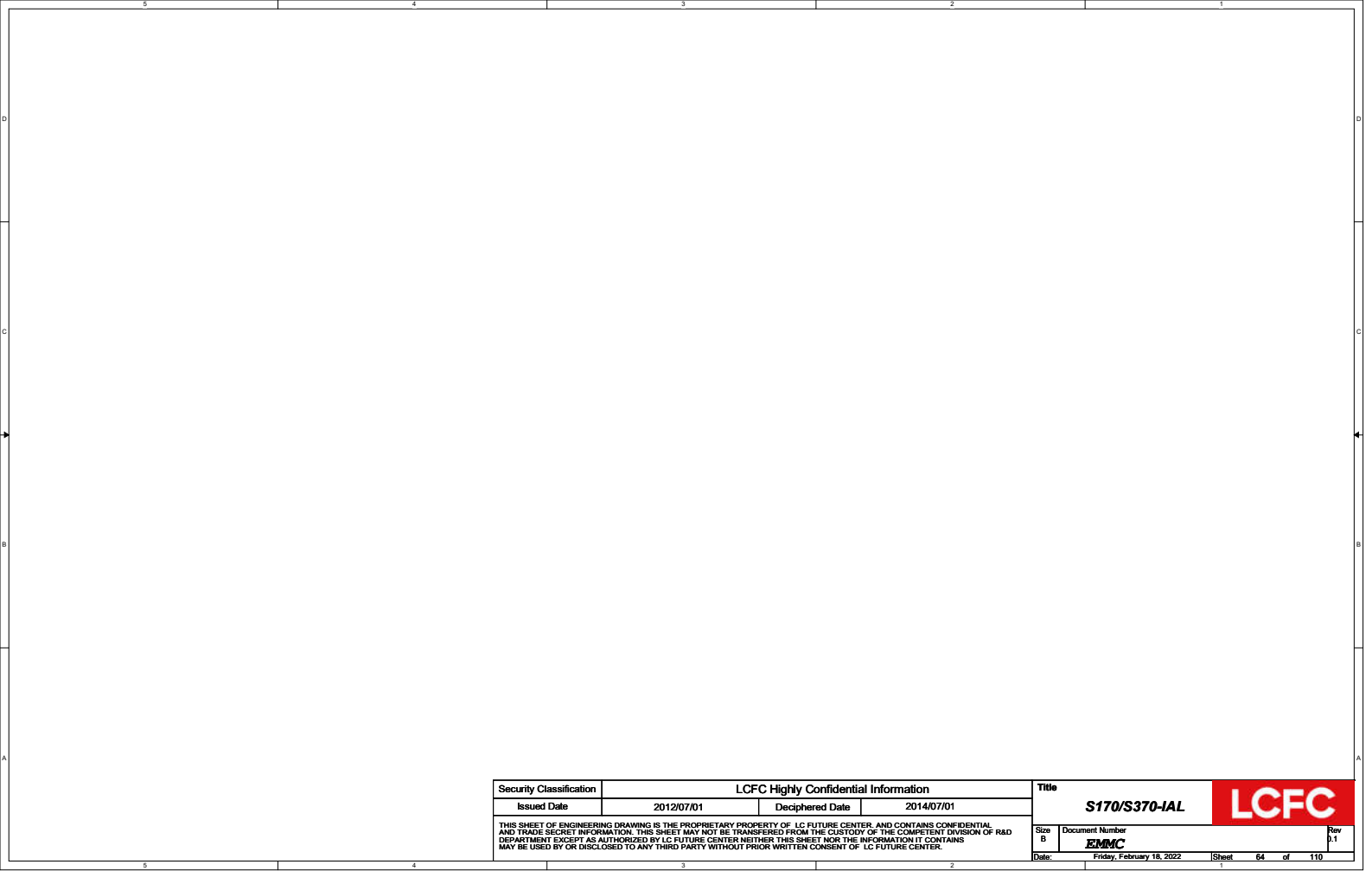
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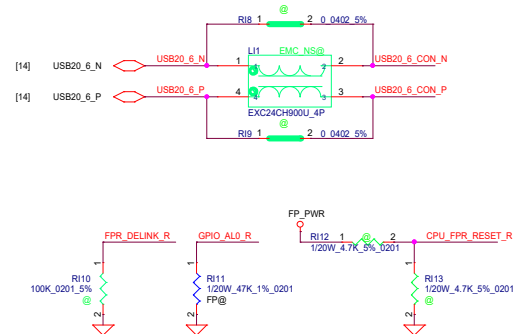
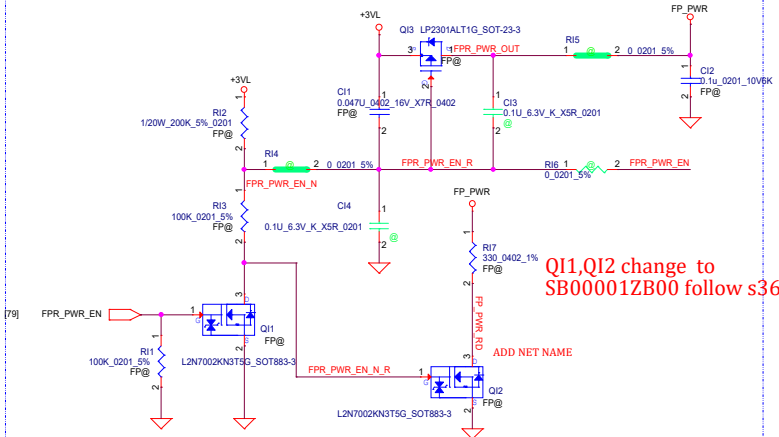


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				EMMC	
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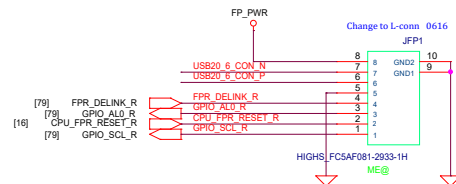
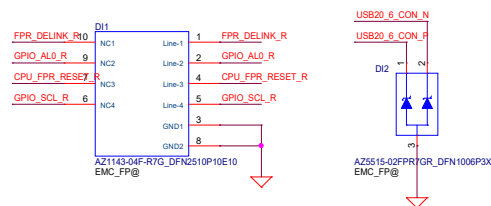


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FP Power Control



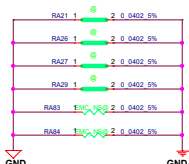
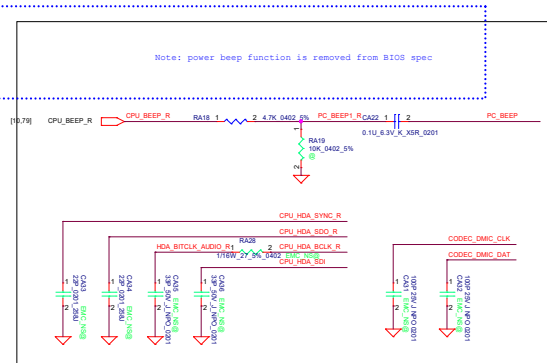
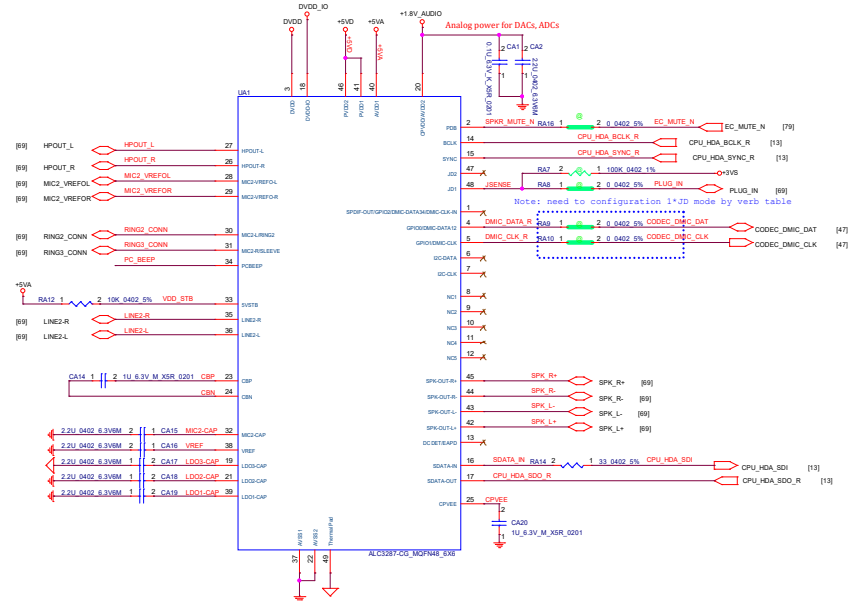
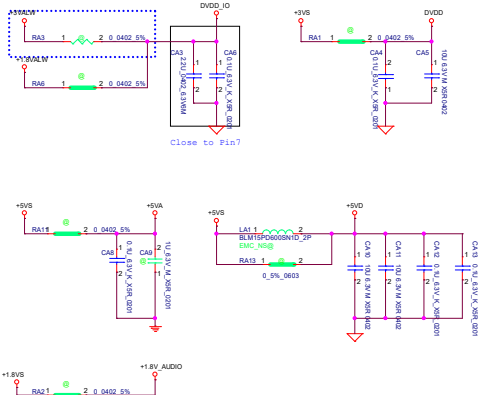
EMC close to Conn

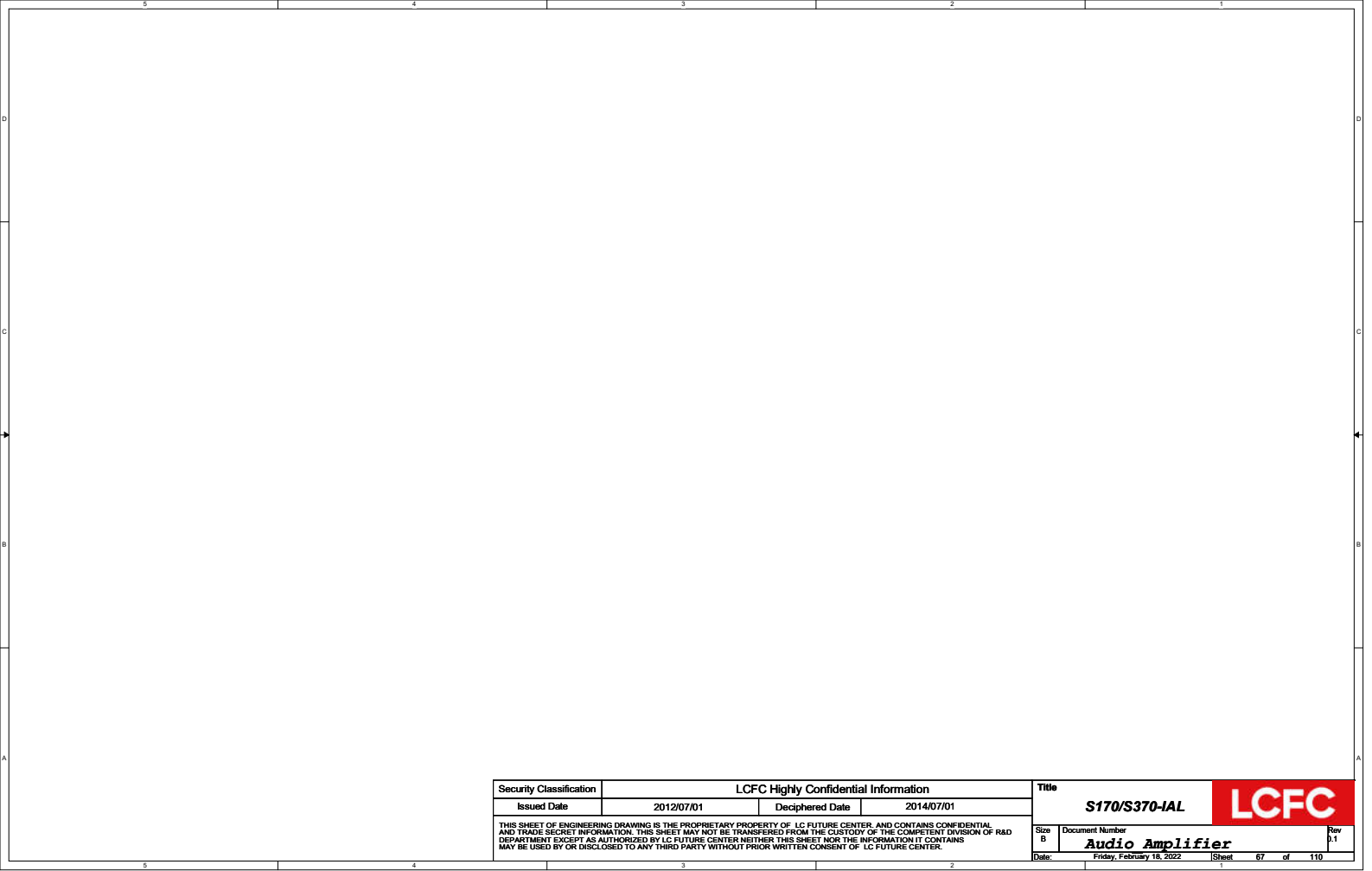


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Size		Document Number						Rev	
		FPR						0.1	
Date:		Friday, February 18, 2022				Sheet 65 of 110			

the different with Base MODULE:
1.Module no ra3 to DVDD_IO,S360&V14&V15 reserve
2.Module no ra5 CA21 to EC_BEEP,S360&V14&V15 reserve
3.RA9&RA10 BOMStructure different with module

Note: DVDD-IO must be equal to or smaller than DVDD



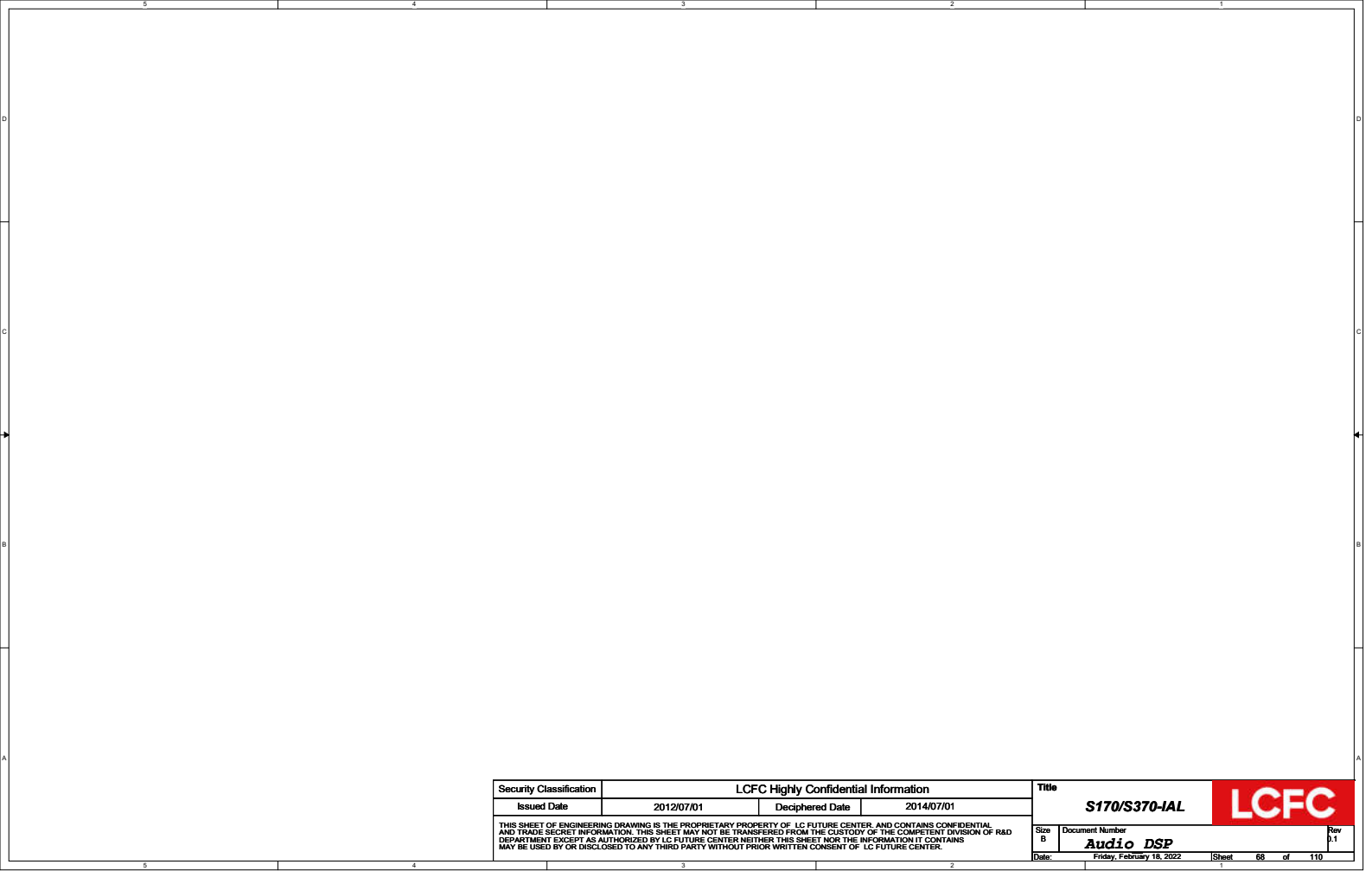


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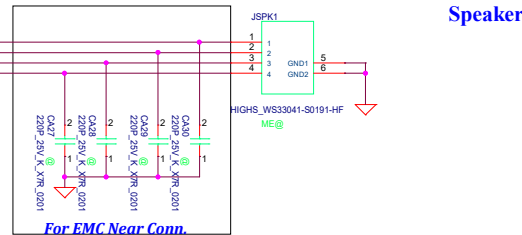
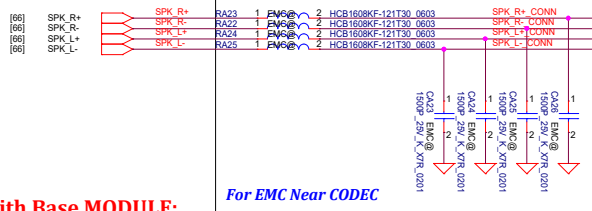


S170/S370-IAL

Audio Amplifier

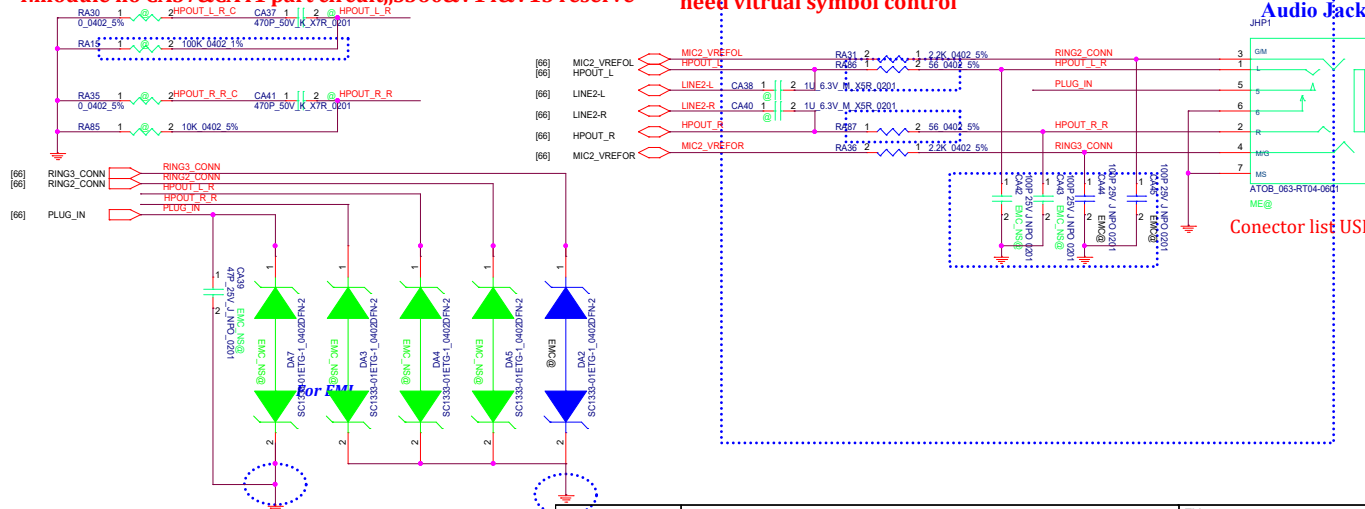


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the diffrent with Base MODULE:

- 1.S360&V14&V15 RA86&RA87 VALUE different with module, Module have RA85&RA88,S360&V14&V15 Remove
- 2.for EMC TVS EMC_NS@ type different with module
- 3.GND type different
- 4.module no CA37&CA41 part circuit,,S360&V14&V15 reserve



Conector list: USE 063-RT04-0701

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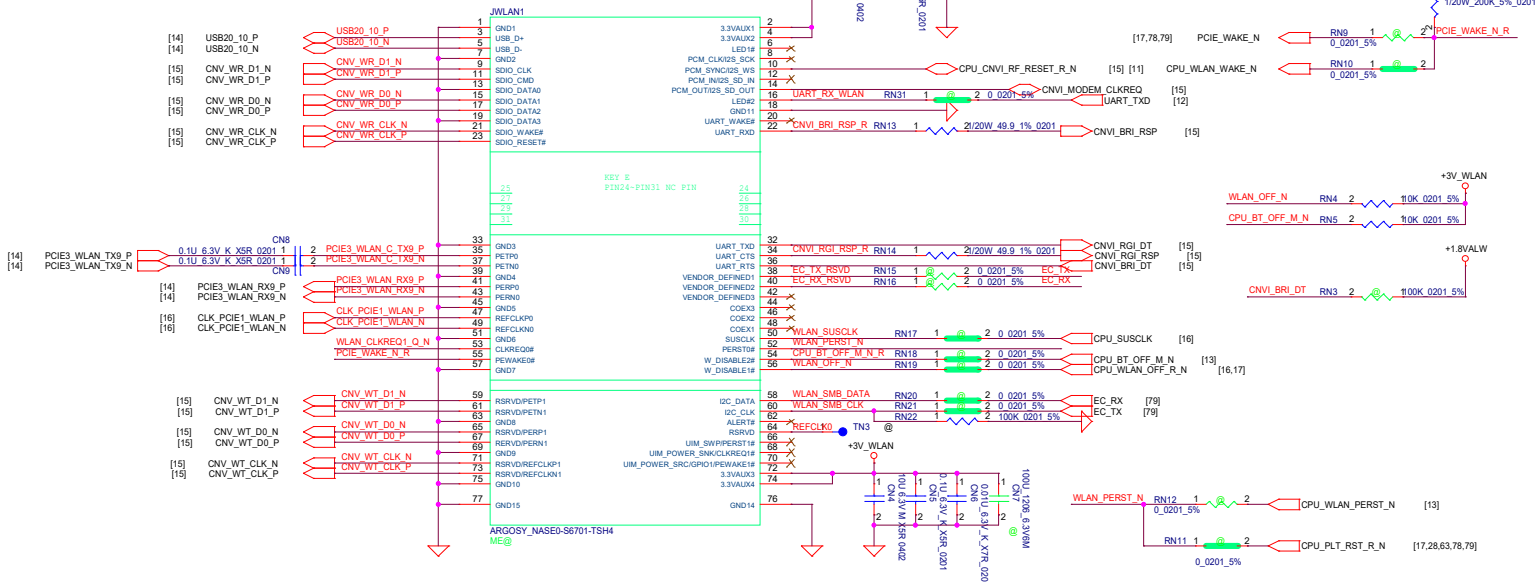
Card reader Circuit MOVE to SUB Board S360


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Size B	Document Number			Rev	
Card Reader				D.1	
Date: Friday, February 18, 2022				Sheet 70 of 110	

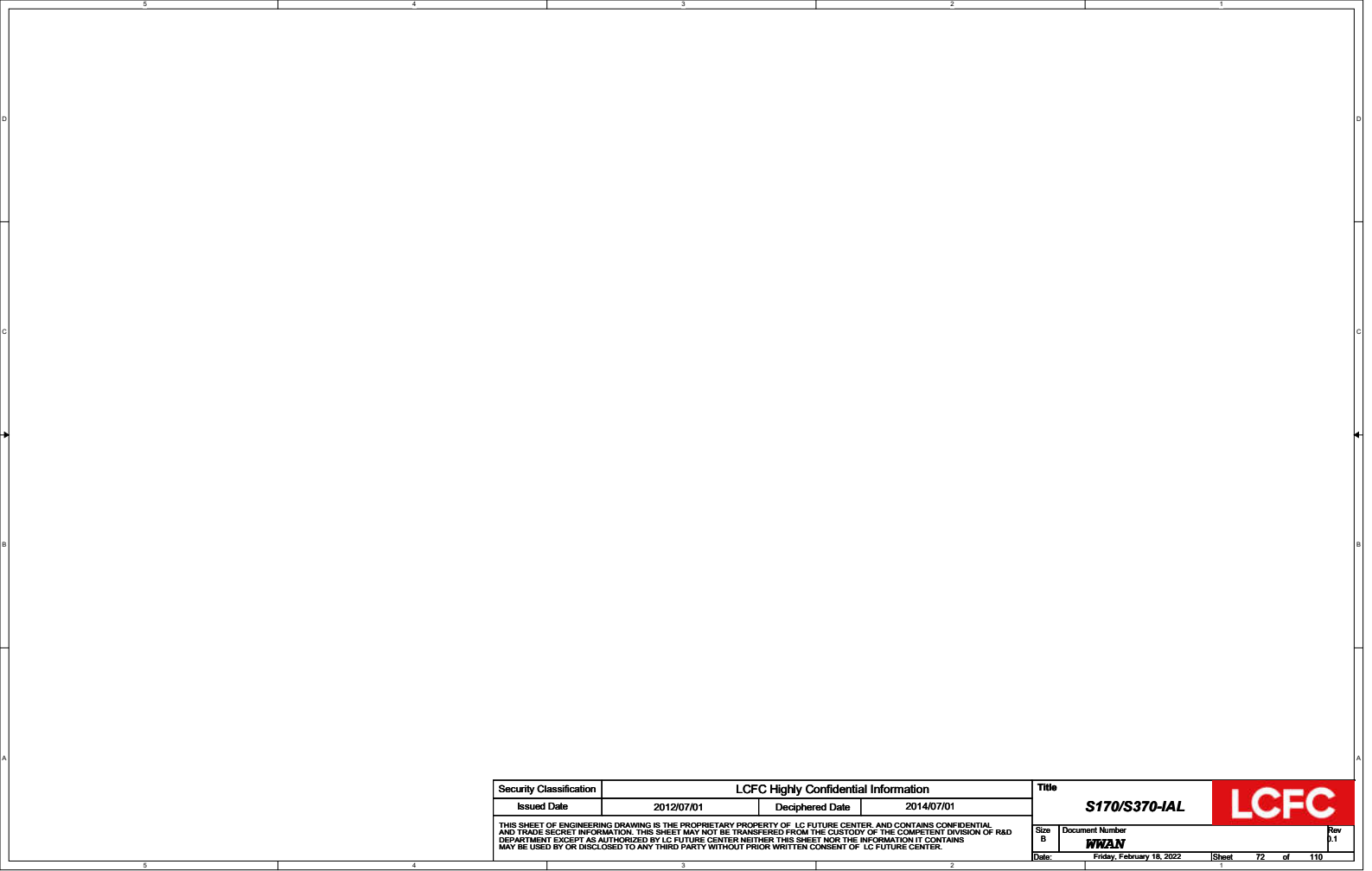
WLAN



```
Signal:CPU_BT_OFF M N
Voltage Level:1.8V
LSI1012XT1G_SC-89-3
Vds max=20V
Vgs max=+/- 6V
Vgs (th)=0.45V/0.9V(min/max)
Rds (ON)=1.25ohm(max,Vgs=1.8 V)
Id=350mA(TA=25 C)
Ton Delay=5ns
```



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LAN Circuit MOVE to SUB Board in V360 DB

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				LAN Chipset		Rev 0.1
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LAN Circuit MOVE to SUB Board in V 14 V15 DB

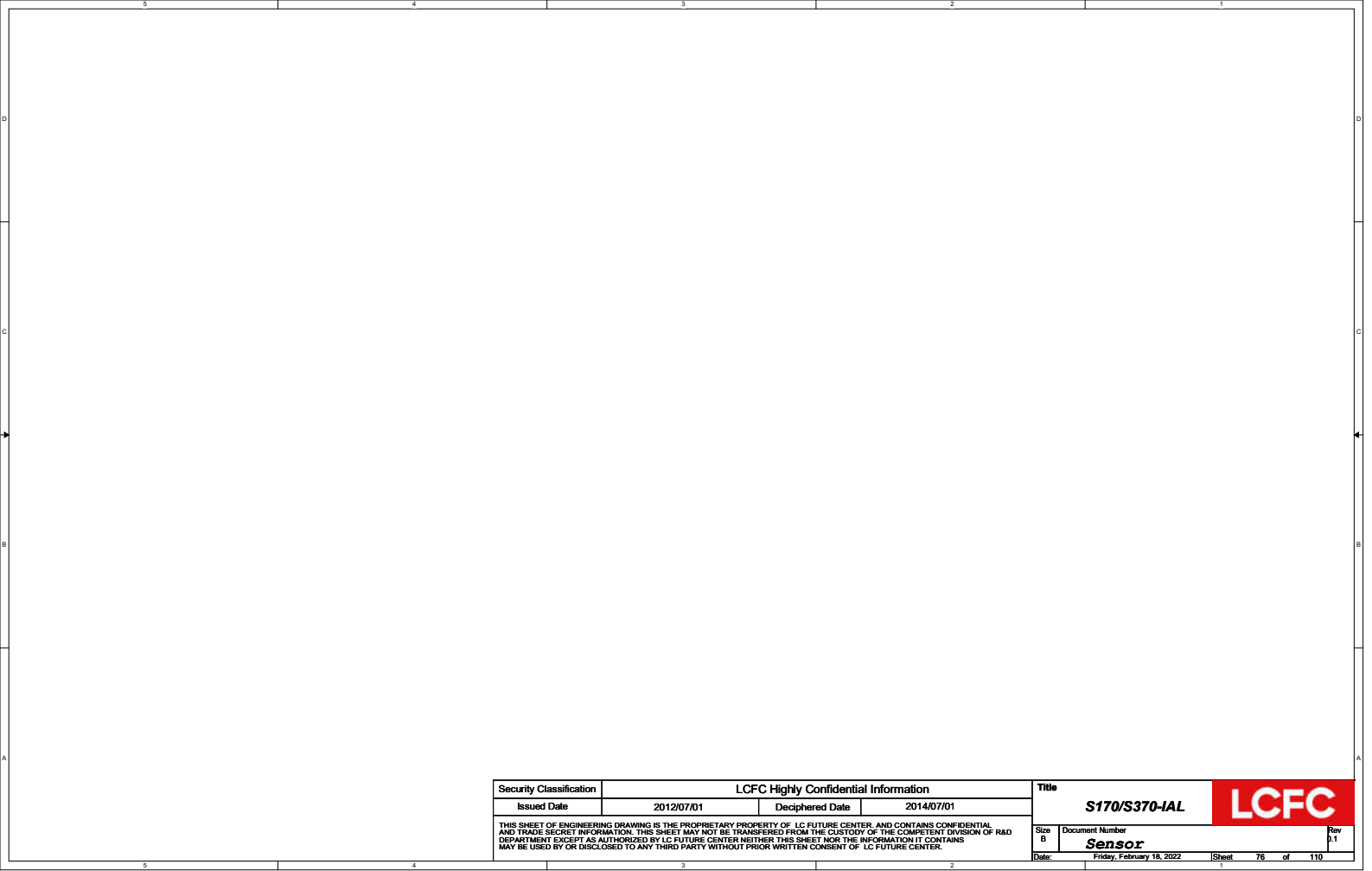
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Size B	Document Number			Rev	
LAN Transformer				D.1	
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LAN Circuit MOVE to SUB Board in V360 DB

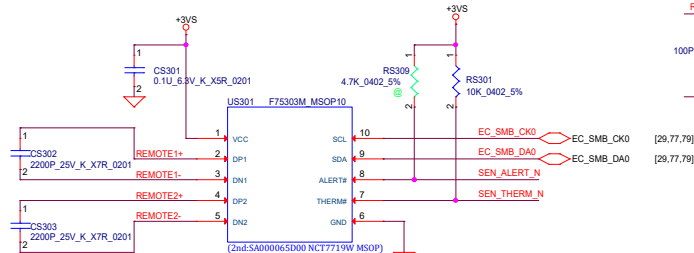
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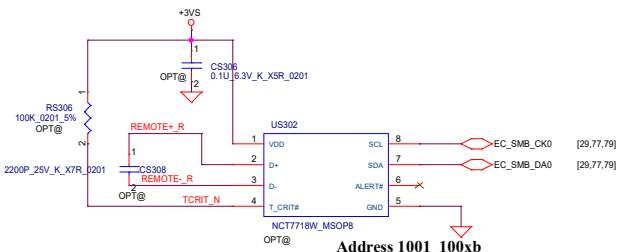
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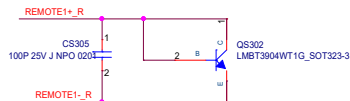
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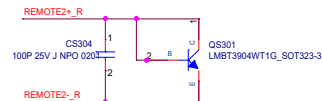
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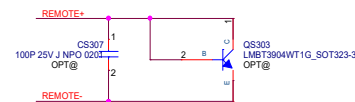
Near CHARGER



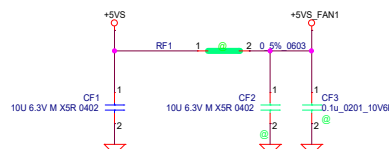
Near CPU



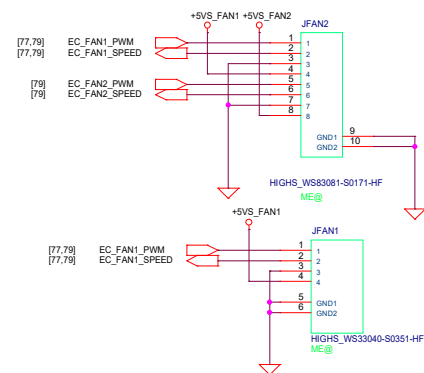
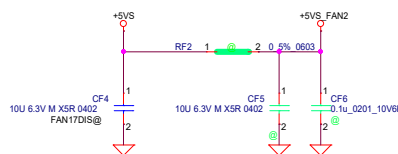
Near GPU



FAN



FAN



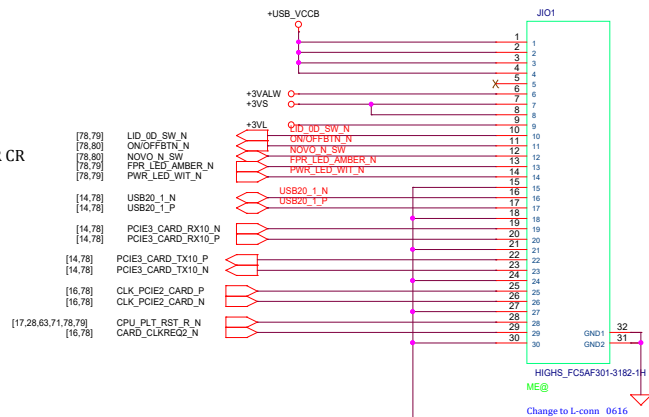
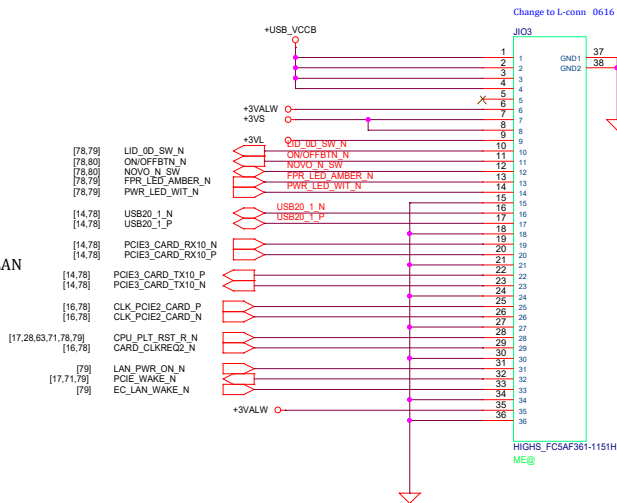
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FPC+cable+Wire

3VALW for LED&V360 Lanchip Power;
3VS for S360 Card Reader, V360 ISOLATE_N

30PIN FOR CR

36PIN FOR LAN

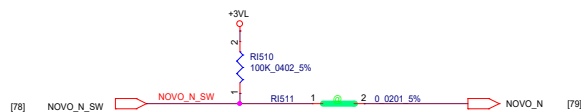


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				Sub Board CONV	
				Date: Friday, February 18, 2022	
				Sheet 78 of 110	

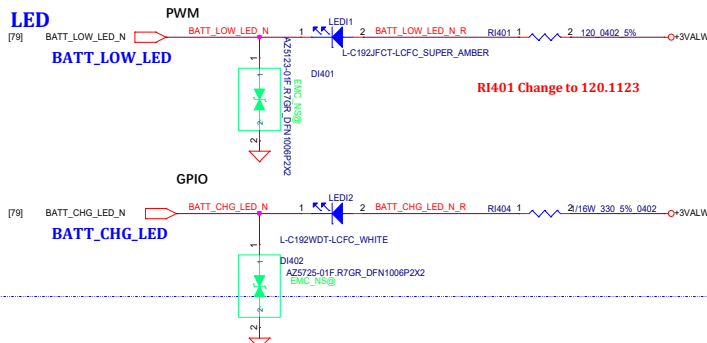
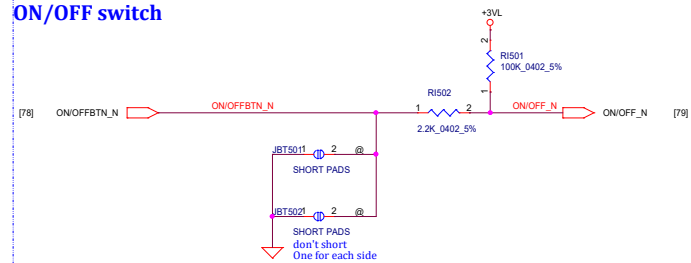
LCFC

Rev 0.1

NOVO switch



ON/OFF switch

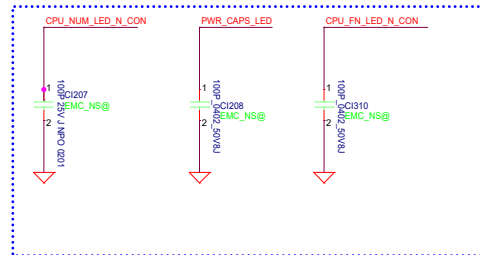
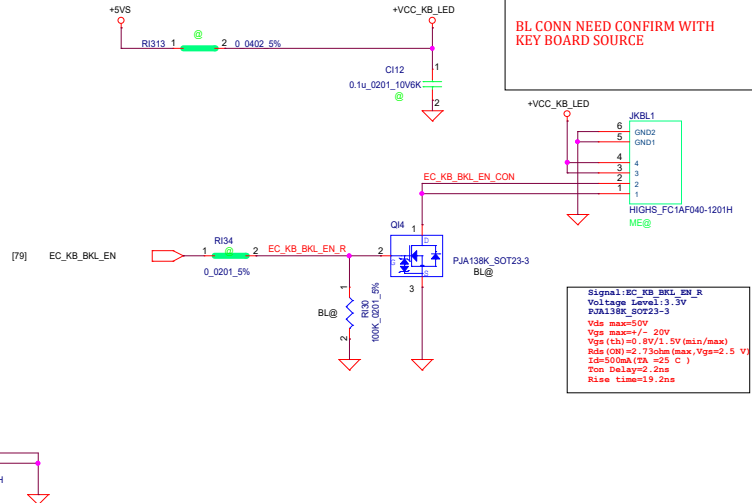



the diffrent with module:
1.module1 mos control LED,S370&V14V15 NO NEED

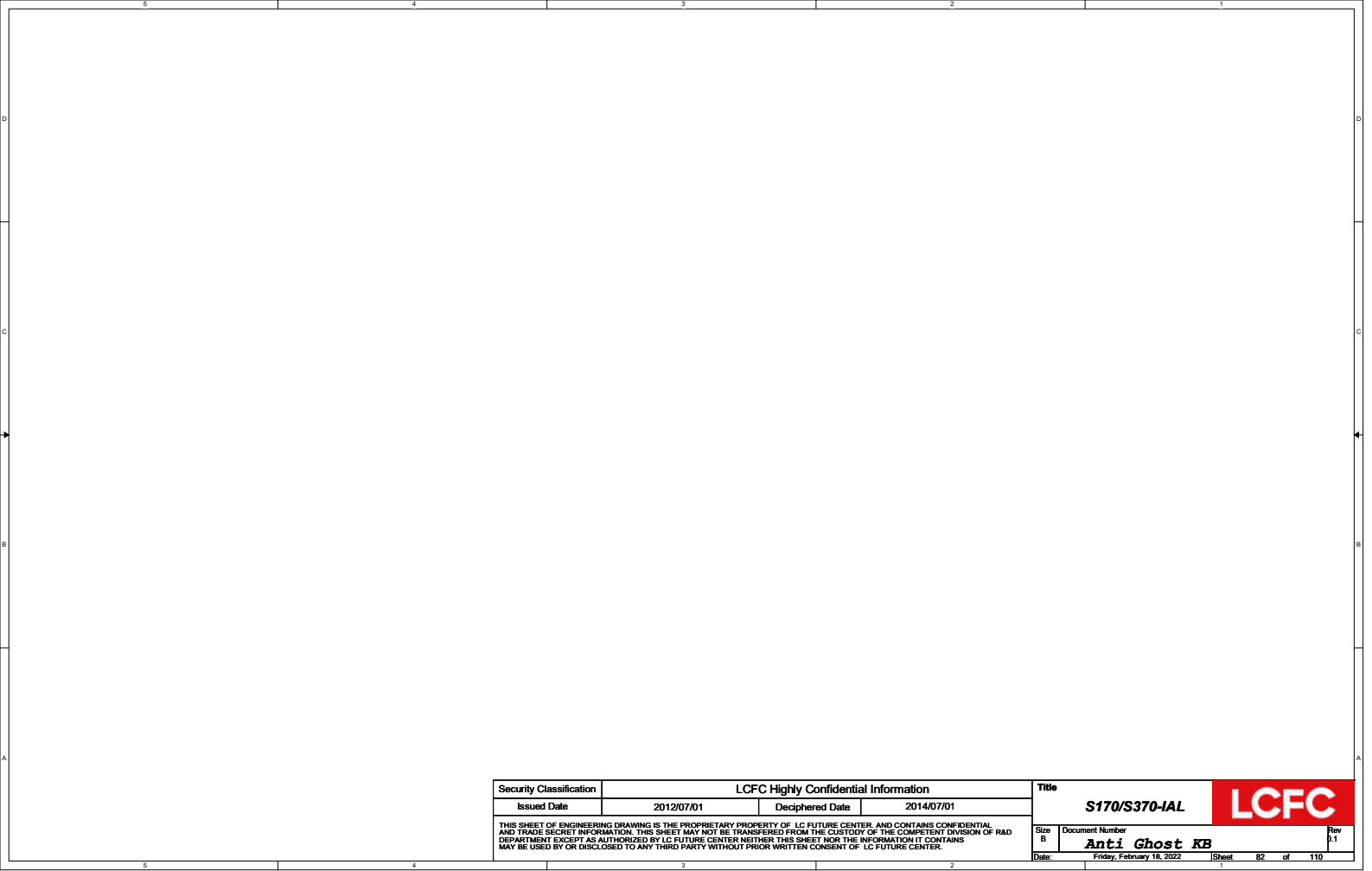
LED	Stute	LED Behavior
Power Button	System on	White_on (battery: 21%-100%)
	Standby LID closed	Amber_on (battery: 0%-20%)
	System off	White_on (battery: 21%-100%)
	Battery only	Amber_Blink_38 (battery: 0%-20%)
Charging	Battery only	OFF
	Charging	Amber_on (battery: 1%-90%) White_on (battery: 91%-100%)

The Power LED move to SUB board LENS

EMC close to Conn



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Date: Friday, February 18, 2022					Sheet 81 of 110



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Date:			Friday, February 18, 2022	Sheet 82 of 110	0.1



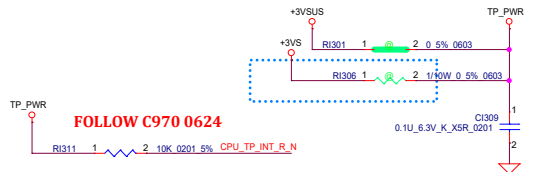
S170/S370-IAL

Anti Ghost KB

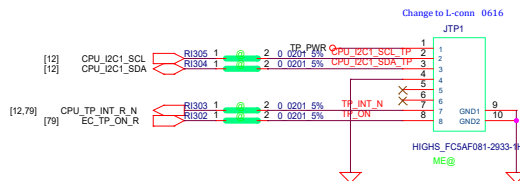
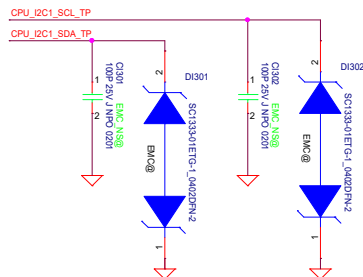
the diffrent with Base MODULE: 1.Module no RI306,S360&V14&V15 Rerserve

Touch Pad

Need support wake up by touch pad
Follow latest UE spec



FOLLOW C970 0624



Change to L-conn 0616

JTP1

HIGH5_FCSAF081-2933-1H

ME@

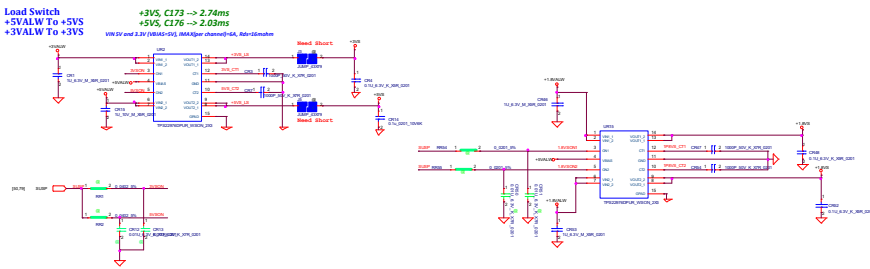
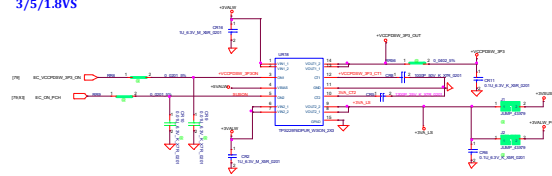
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				TouchPad CONN	
				Date: Friday, February 18, 2022	
				Sheet 83 of 110	

LCFC

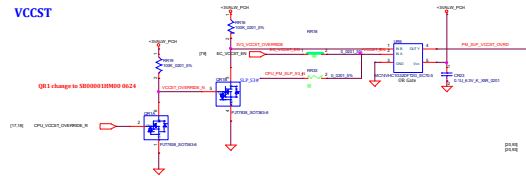
Rev 0.1

Load Switch
+5VALW To +5VS +3VS, C173 → 2.74ms
+3VALW To +3VS +5VS, C176 → 2.03ms

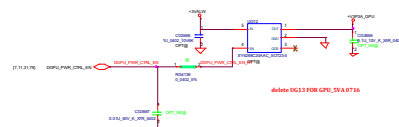
VIN 5V and 2.1V (VBIAS=5V), IMAX(per channel)=6A, Rds=26mohm



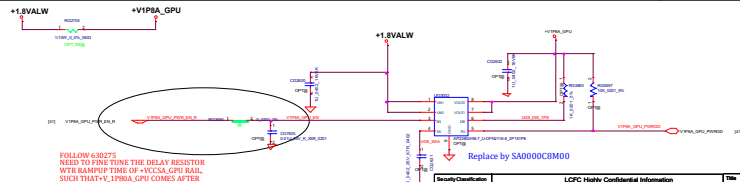
VCCST EN Signal modify 0624



+3VALN to +3V_GPU

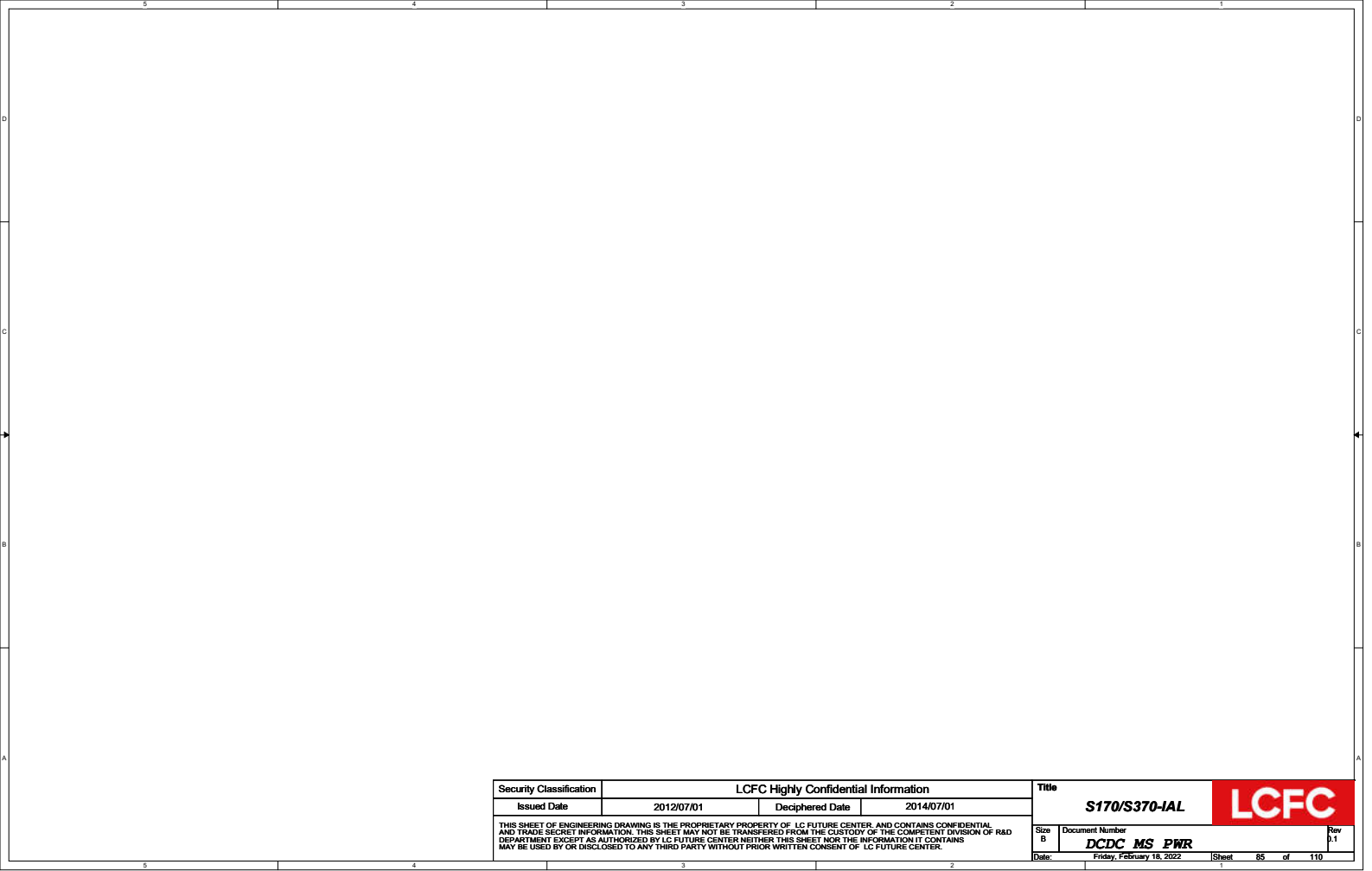


+1.8VALW +V1P8A



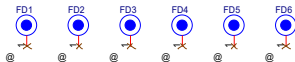
FOLLOW 630275
NEED TO FINE TUNE THE DELAY RESISTOR
WTR RAMPUP TIME OF +VCCSA_GPU RAIL,
SUCH THAT +V_1P80A_GPU COMES AFTER
+VCCSA_GPU RAIL.

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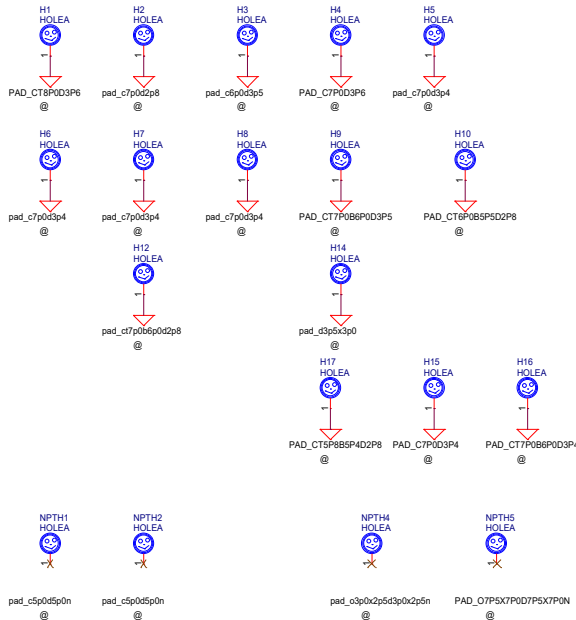


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Size B	Document Number				Rev
	DCDC MS PWR				0.1
Date:	Friday, February 18, 2022			Sheet	85 of 110

PCB Federal Mark PAD

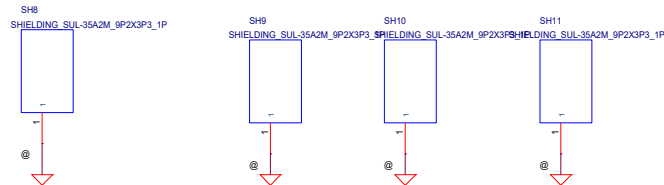


Hole



MD Shielding

SO-DIMM Shielding



Security Classification

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Title

Issued Date

2012/07/01

Deciphered Date

2014/07/01

S170/S370-IAL

LCFC

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Size B

Document Number

Date:

Friday, February 18, 2022

Sheet

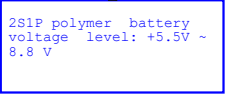
66

of

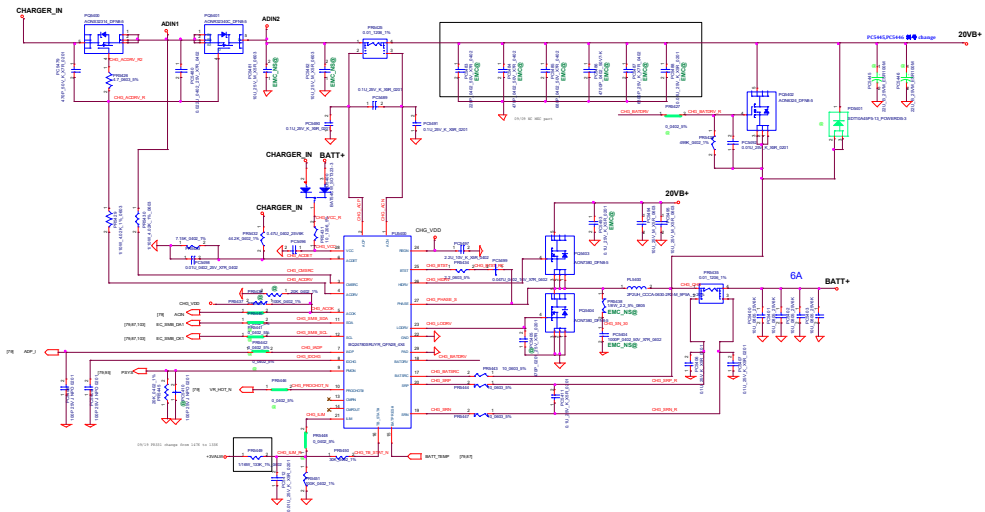
110

Rev

0.1



LCFC



ACDC2 setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =20A
 Discharge current limit HW=9A during Turbo boost

IDPM	V(ILIM)	PR5320
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K
4.0A	2.6V	162K

$V(ILIM)=1V+40x(VACP-VACN)=1+40xIDPMxRAC$

← LOGIC

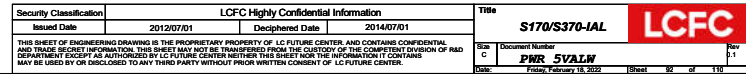
END IN USE	PR5333
1uH	93K
2.2uH	137K
3.3uH	169K

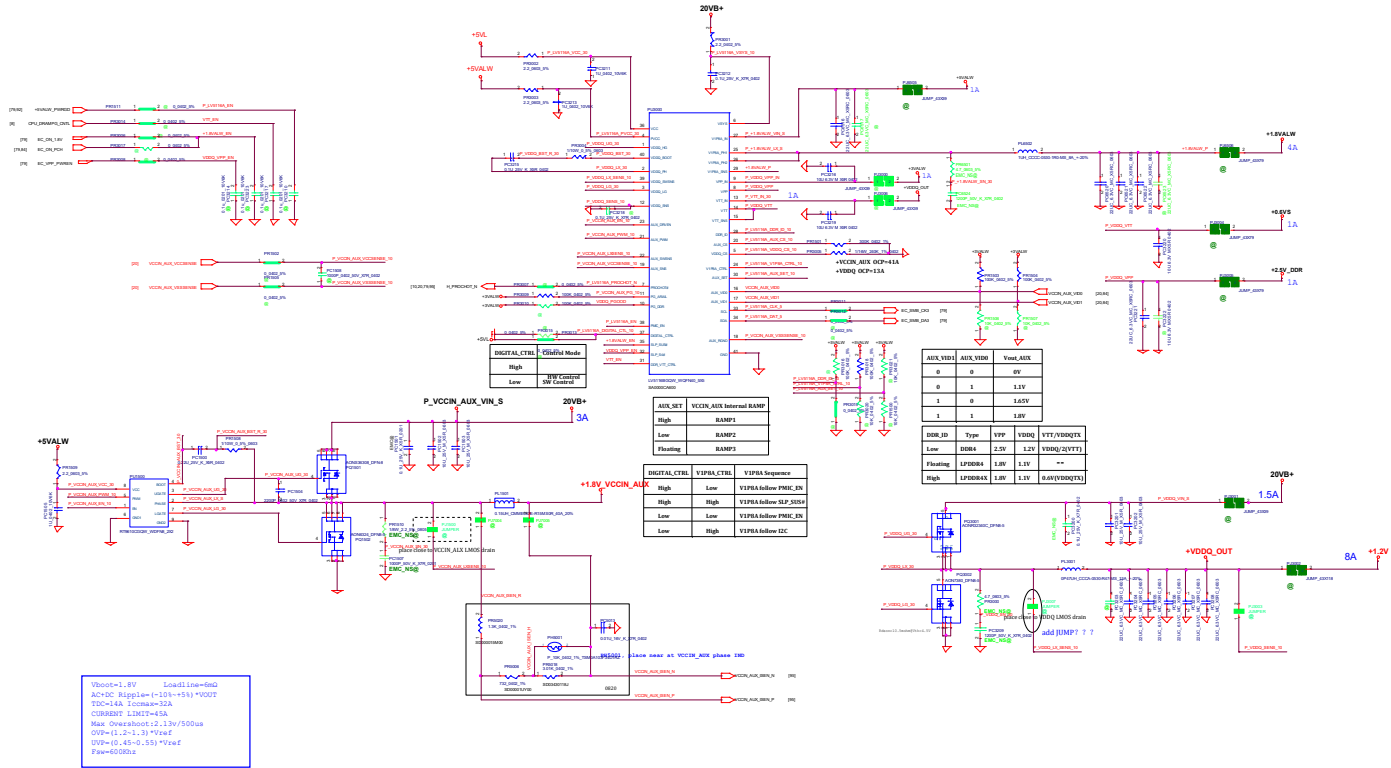
← LOGIC

# of CELL	VCELL_PRES	PR5322
1-CELL	1.5V	301K
2-CELL	2.4V	150K
3-CELL	3.3V	82K
4-CELL	4.5V	33.2K

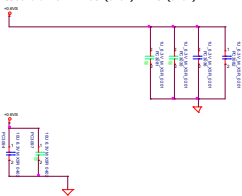
← LOGIC

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Rev		Document Number		LCFC	
C		P090-PWR DCC--NA		Rev 1.0	
Date:		Friday, February 18, 2023		Sheet 90 of 119	

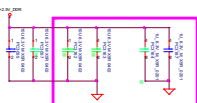




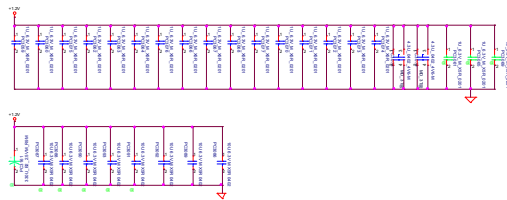
VTT
PDG 2 Channel SODIMM: 2*10UF(0603,1 placeholder)+4*1UF(0402)
S360: channel A:1*10UF(0402)+ 2*1UF(0201)



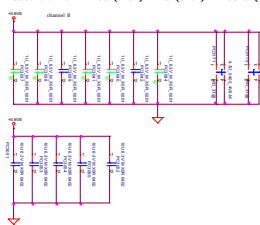
VPP
PDG 2 Channel SODIMM: 2*10UF(0603)+2*1UF(0402)
S360: channel A:1*10UF(0402)+ 1*1UF(0201)



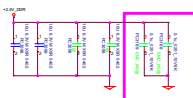
VDDQ
PDG2 Channel SODIMM: 1*330UF(7343)+16*10UF(0603)+16*1UF(0402)
S360: channel A:8*10UF(0402)+ 16*1UF(0201)



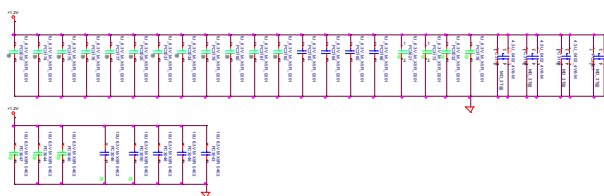
VTT
PDG 2 Channel MD: 4*10UF(0603)+16*1UF(0402)
S360: channel B:2*10UF(0402)+ 2*1UF(0201)+2*4.3UF3T(P24)



VPP
PDG 2 Channel MD: 5*10UF(0603)+16*1UF(0402)
S360: channel B: 2*10UF(0402)+8*1UF(0201)(P26)



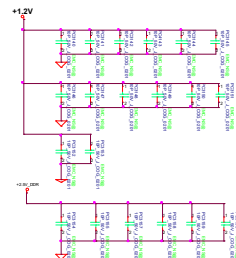
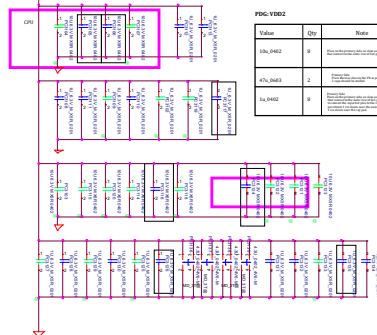
VDDQ
PDG 2 Channel MD: 10*10UF(0603)+32*1UF(0402)
S360: channel B:5*10UF(0402)+4*1UF(0201)+3*4.3UF3T

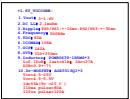


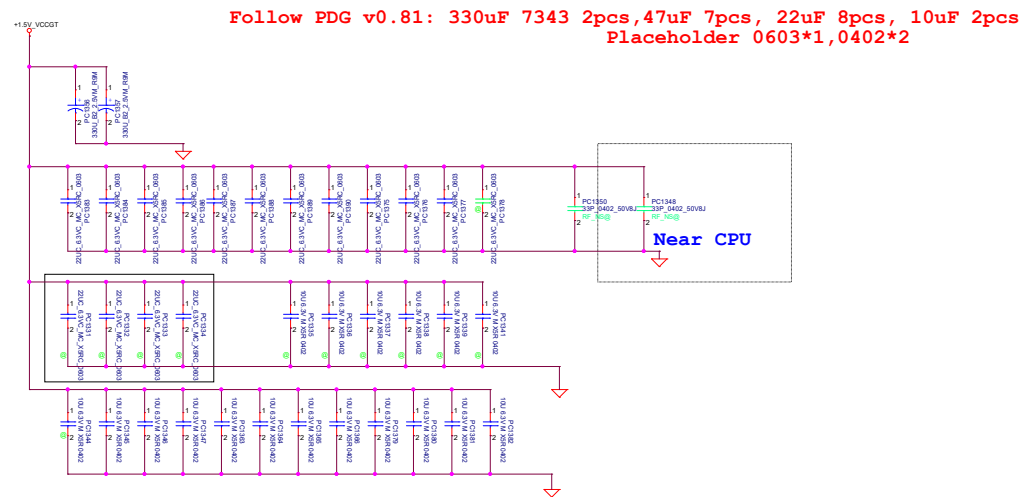
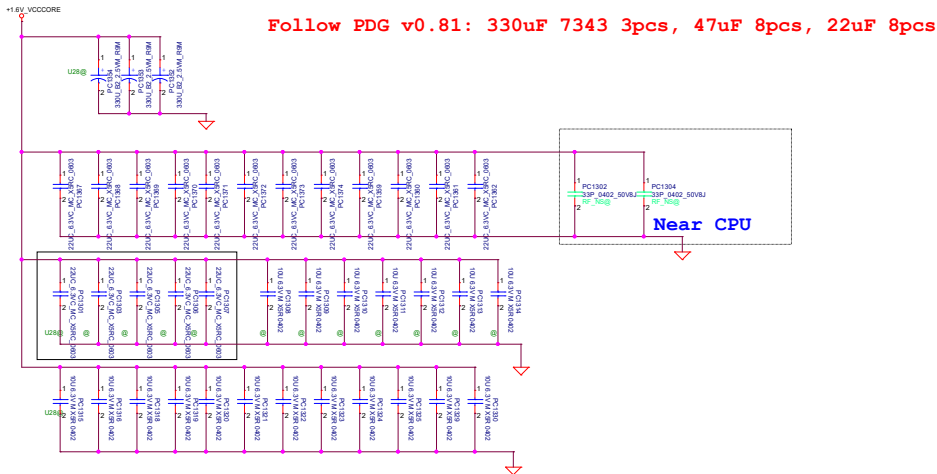
VDD2
+1.2V PDG: 2*47UF(0603)+ 8*10UF(0402)+8*1UF(0402)
S360: 4*22UF(0603 P93)+ 6*10UF+9*1UF

CHANGE VDD2 MLCC 0625

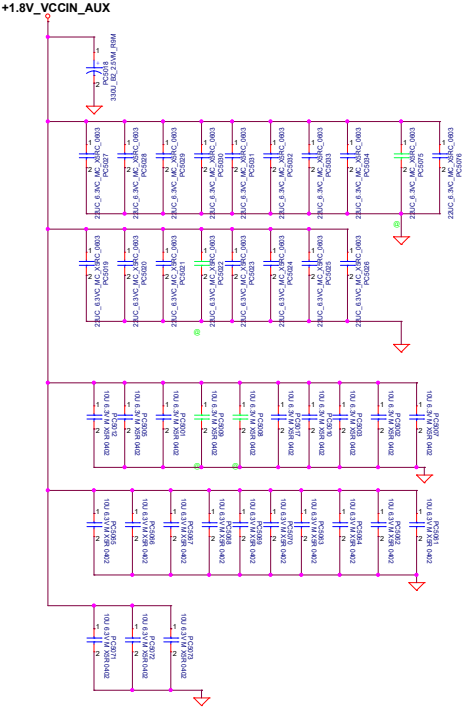
Value	Qty	Note
10h_0402	8	Place on the primary side as close as possible to the one that contains the feedback loop of the first stage
47u_0603	2	Primary Side Place 47uF electrolytic filter capacitor on the positive output of the boost converter
1u_0402	8	Primary Side Place 1 uF on the primary side as close as possible to the one that contains the feedback loop of the first stage, one capacitor is located on the secondary side of the first stage, one capacitor is located on the secondary side of the second stage, one capacitor is located on the output of the second stage and one capacitor is located on the output of the third stage

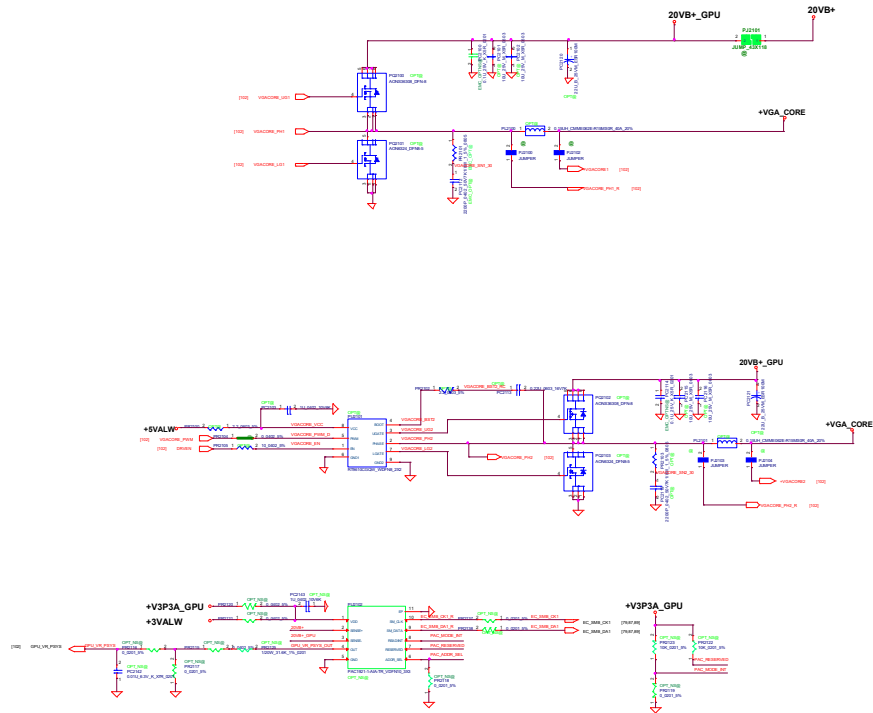






Follow PDG v0.81:330uF 7343 1pcs, CPU side 47uF*8, 10uF 10pcs

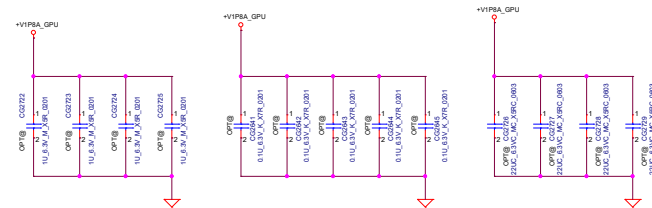




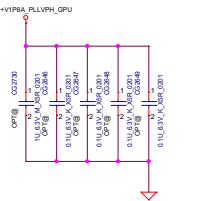
VGA_CORE
Vboot=0V
Ripple=120mV
TCC=40-1A Iccmax=62A
OCP=90A
L2=20mohm
Fsw=600KHz

Reference design 1210nf_0528
C770-1210nf

+V1P8A_GPU RAIL



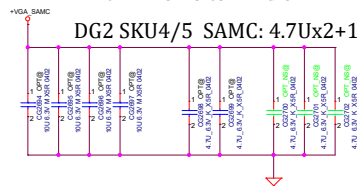
+V1P8A_PLLVPH RAIL



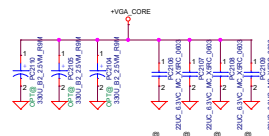
GPU DECOUPLING: VCCSAMC_GPU

SECONDARY SIDE
TO BE PLACED CLOSE THE GPU

DG2 SKU4/5 SMC: 4.7Ux2+10Ux4

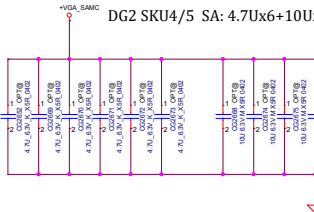
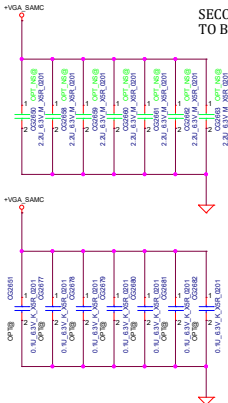


TO BE PLACED NEAR THE VREG



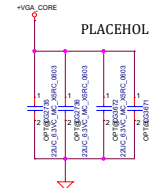
SECONDARY SIDE
TO BE PLACED CLOSE THE GPU

DG2 SKU4/5 SA: 4.7Ux6+10Ux4

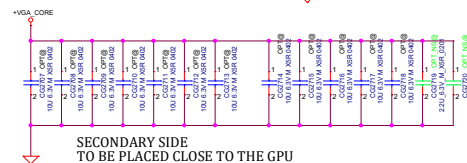


PRIMARY SIDE

PLACEHOLDER (FOR SOCKET COMPENSATION)



Follow AEP



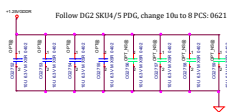
SECONDARY SIDE
TO BE PLACED CLOSE TO THE GPU

GPU GDDR DEVICE DECOUPLING

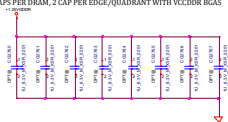
4 CAPS PER DRAM, 1 CAP PER EDGE/QUADRANT WITH VCCDDR & VCCDDRQ BGAS



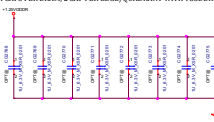
Follow DG2 SKU4/5 PDG, change 10u to 8 PCS: 0621



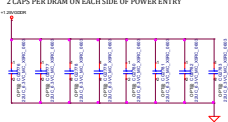
4 CAPS PER DRAM, 2 CAP PER EDGE/QUADRANT WITH VCCDDR BGAS



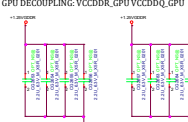
4 CAPS PER DRAM, 2 CAP PER EDGE/QUADRANT WITH VCCDDRQ BGAS



2 CAPS PER DRAM ON EACH SIDE OF POWER ENTRY

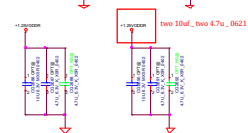


GPU DECOUPLING: VCCDDR_GPU VCCDDQ_GPU



SECONDARY SIDE
TO BE PLACED CLOSE TO GPU

Change 2.2u to 4.7u



Change List

- 1.RC265 change to 0201 for ME request
 - 2.ADD RG4155 for DGPU_PERST_N shutdown glitch,RG3855 no stuff
 - 3.RC168,RC169 change to 0201/1%
 - 4.PC7925(0.22U) change to CG7925(0.01U) ,PC7927(0.22U) change to CG7927(0.01U)
 - CG2631 change to 0.022U, RG2694 change to 0ohm
 - 5.RG4147 change to 10K, ADD RG4154 ,ADD DG1800
 - ADD RG4156
 - 6.ADD BU120,BU121,RU122,RU123 FOR S170
 - 7.RC314 no stuff
 - 8.RU32 change to 23.7K, DELETE CU7,CU8,CU121 stuff
 - 9.delete UG7,RG121 RG4138,ADD CG927,DG231,QG3529,QG3530,RG121,RG4138,RG4157
- 11/22
- 1.GPP_E22, ADD 10K PULL DOWN RSVD
- 11/23
- 1.RI206,RI213Change to 0ohm
- 12/06
- 1.F28,PEG_RST_Npull high to V3P3AGPU,PEG_RST_M1_N pull high to 1.8VALW_PCH
 - 2.RI101,RI102change to 0ohm

- 1.del PR2059
- 2.ADD PC5075,PC5076
- 3.GPU PWR conntroller VCC PVCC change to +5VS,PR2060 stuff,PR2061 no stuff
- 4.DCIN_ATTACHED_EC change to pull high to +3VL ,PQ202 SWAP,PR206 change to 499K
- 5.PR2214 change to 0 ohm
- 6.ADD PC2110, ADD PR2062,PR2063,PR2041 ,PR2045change to 698ohm
- 7.PR2031 change to 23.7K,PR2032 change to 12.7K
PR2033 change to 16.9K,PR1068 change to 31.6K
PR1069 change to 26.7K,PC1015 change to 56PF
PR1078 change to 10.5K,PR2039 change to 30.1K
PR2056 change to 73.2K,PR2058 change to 100K
CG2717,CG2718,CG3671,CG3672 stuff
- 8.CPU power电感换2.4mm高的sample: PL1101,PL1102,PL1201,PL1501并增加相应的short pin
- 9.非core power的电感主料换Coilforce的PN(PL6502,PL3001,PL5701,PL5400,PL5601)
- 10.PQ 1102,PQ1104,PQ1106,PQ1108,PQ1202,PQ1204,PQ1502 change to AON6324

11/23

- 1.PR2033 16.9K change to 11.3K
- PR2031 23.7K change to 21K
- PR2032 12.7K change to 15.4K
- PR2039 30.1K change to 95.3K
- PC2005 220P change to 150pF
- PR2028 470 change to 402R
- PR2015 2.37K change to 6.19K
- PR2024 1K change to 3.32K
- PR2027 442 change to 49.9R


11/25

- 1.PC2202,PC2224,PC4002,PC4003,PC4019,PC4020,
PC5494,PC5495,PC5601,PC5604,PC5703,PC5704
change to SE000010U00
- 2.Delete PJ1501,PJ1100,PJ1101,PJ1200 ,delete PD2000

12/13

- 1.P103: delete PJ2101,ADD PR2130,PR2131,ADD PU2102及其周边相关电阻电容,
- 2.P104: 20VB+ change to20VB+ _GPU

2022/02/08
1.PJ2201 Change to PL2202

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